Turboelectric Aircraft DC Network Fault Analysis and Protection Solution using Superconducting Fault Current Limiters

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Hamoud Alafnan

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Department of Electrical and Electronic Engineering
University of Bath

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Abstract

Excluding the strong impact of COVID-19 on the aviation sector, the annual increase in aircraft passengers and freight traffic were estimated to be around 6.4% and 4.2%, respectively, according to the International Civil Aviation Organization (ICAO). According to the United States Environmental Protection Agency (EPA), the transportation sector is the US's largest source of carbon dioxide (CO_2) emissions at 28%, and will only dramatically increase with current aviation technologies.

The National Aeronautics and Space Administration (NASA) in the US and the Advisory Council for Aviation Research and Innovation in Europe (ACARE) have set goals to limit atmospheric pollution and reduce greenhouse gases. The environmental goals of NASA and ACARE are the reductions of CO_2 by 75%, NOx by 90% and external noise by 65% relative to their levels in 2000; targets which are unfeasible using traditional aircraft design due to the relatively low efficiencies. To achieve these goals, aircraft, including the propulsion system, must work with superior efficiency.

The turboelectric distributed propulsion (TeDP) system is considered one of the best approaches for future large-scale aircraft to achieve the desired environmental goals. The main idea of the TeDP system is to replace the traditional turbofan/combustion engine with a turboshaft that runs electric generators connected to electric motors via a DC microgrid, which includes converters to control motors/propellers to produce the thrust required by the aircraft.

The merging of electrical components in turboelectric aircraft (TeA) and the installation of onboard electrical power systems offer several design opportunities for optimization and system improvement. However, there are several design challenges for the TeA system, including protecting the DC distribution system against faults. It is

a significant challenge due to the high magnitude of fault currents, the absence of zero-crossing points, low line impedance and high bus voltage (6 kVDC). As the expected fault currents have a high magnitude and a short rise time in the airborne DC microgrid, and DC circuit breakers (CBs) have long operation times of up to 4 msec, the need for a device to limit fault currents and ensure safe operation of the CBs is inevitable.

In this thesis, one set of the TeA is modelled in MATLAB®/Simulink environment to conduct the DC fault analysis, with results indicating that fault currents are extremely high in pole-to-pole and pole-to-ground with low grounding impedance faults. Based on the DC fault analysis results, a multilayer thermoelectric resistive superconducting fault current limiter (r-SFCL) is modelled to reduce the fault currents and support the protection system. The multilayer thermoelectric r-SFCL is tested with different copper stabilizers and shunt resistors. The best candidate model, in terms of fault current limiting capability and recovery time, is integrated into the power protection system to reduce the fault current in the time gap between the fault occurrence and the fault clearance. The nominated r-SFCL model was successfully able to reduce the prospective fault currents by up to 80% for up to 64 msec without reaching a permanently damaging temperature (400 K). Finally, a controlled superconducting magnetic energy storage (SMES) is integrated into the TeA power system architecture to supply the propulsion system during a short period of temporary power loss.

This thesis provides an effective and embeddable r-SFCL model which considers the electrical and thermal behaviour of each layer in the superconductor tape as well as the heat transfer between the r-SFCL and the coolant, liquid nitrogen (LN_2). The robust model presented in this thesis can help with the protection planning for power-dense electrical networks such as those in TeA.

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List of Publications

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- **H. Alafnan**, M. Elshiekh, X. Pei, S. Altouq, S. Fazeli, Q. Sun, M. Zhang, W. Yuan., "Application of SMES-FCL in Electric Aircraft for Stability Improvement," *IEEE Trans. Appl. Supercond*., vol. 29, no. 5, pp. 1–6, 2019, doi: 10.1109/TASC.2019.2905950. (Appendix B)

- **H. Alafnan**, X. Zeng, X. Pei, M. Khedr, M. Zhang, and W. Yuan, "Analysing Faults and SFCL Response in Electric Aircraft," *J. Phys. Conf. Ser.*, vol. 1559, no. 1, 2020, doi: 10.1088/1742-6596/1559/1/012103. (Appendix C)

- Q. Sun, D. Xing, **H. Alafnan**, X. Pei, M. Zhang, and W. Yuan, "Design and test of a new two-stage control scheme for SMES-battery hybrid energy storage systems for microgrid applications," *Appl. Energy*, vol. 253, 2019, doi: 10.1016/j.apenergy.2019.113529.

- M. Elshiekh, **H. Alafnan**, A. Elwakeel, X. Pei, S. Venuturumilli, W. Yuan, M. Zhang, "Utilising SMES-FCL to improve the transient behaviour of a doubly-fed induction generator DC wind system," *Int. J. Electr. Power Energy Syst.*, (under review).

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List of Abbreviations

AC	Alternating Current
ACARE	Advisory Council for Aviation Research and Innovation in Europe
AEA	All-Electric Aircraft
APU	Auxiliary Power Unit
BSCCO	Bismuth Strontium Calcium Copper Oxide
CB	Circuit Breaker
CD	Current Differential (Fault Detection Method)
CO_2	Carbon Dioxide
CSC	Current Source Converter
CFRP	Carbon Fiber Reinforced Polymer
DC	Direct Current
DEAP	Distributed Electrical Aerospace Propulsion
EP	Electric Propulsion
EPA	Environmental Protection Agency
ESN	Electrical Structure Network
FBW	Fly by Wire
FOC	Field-Oriented Control
HEA	Hybrid Electric Aircraft
HTS	High-Temperature Superconductors
IATA	International Air Transport Association
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated-Gate Bipolar Transistor
i-SFCL	Inductive Superconducting Fault Current Limiter
LCS	Load Commutation Switch
LTS	Low-Temperature Superconductors
LVDC	Low-Voltage Direct Current
MVDC	Medium-Voltage Direct Current
MOV	Metal-Oxide Varistor

MMC	Modular Multilevel Converter
NASA	National Aeronautics and Space Administration
NPC	Neutral-Point Clamped
OC	Overcurrent Detection (Fault Detection Method)
PLL	Phase-Locked Loop
PWM	Pulse-Width Modulation
r-SFCLs	Resistive Superconducting Fault Current Limiter
SFCL	Superconducting Fault Current Limiter
SPMSM	Surface Permanent Magnet Synchronous Motors
SOC	State of Charge
SMES	Superconducting Magnetic Energy Storage
TeA	Turboelectric Aircraft
TeDP	Turboelectric Distributed Propulsion
UAV	Unmanned Aerial Vehicle
UFD	Ultra-Fast Disconnector
UV	Under-Voltage
VSC	Voltage Source Converter
VFDs	Variable Frequency Drives
YBCO	Yttrium Barium Copper Oxide

Chapter One

1. Introduction

1.1 Thesis background

Until the COVID-19 pandemic occurred, the aviation sector has seen continuous growth worldwide [1]. Fig. 1.1 shows the trends in world passenger traffic from 1945 to 2020, in which the world witnessed several global-scale events that slowed the sector's growth, such as the Gulf war in 1991, the September 11 attacks in 2001, the great recession of 2008-2009 and the COVID-19 pandemic in 2020 [1]. With COVID-19, the aviation sector's recovery may take longer compared to previous events, but it should witness growth again based on historical trends. In 2019, 4.54 billion passengers were carried by aircraft – a 3.76% increase compared to 2018 passenger numbers [2]. Passenger numbers are estimated to hit 8.2 billion by 2037 according to the International Air Transport Association (IATA) [3].

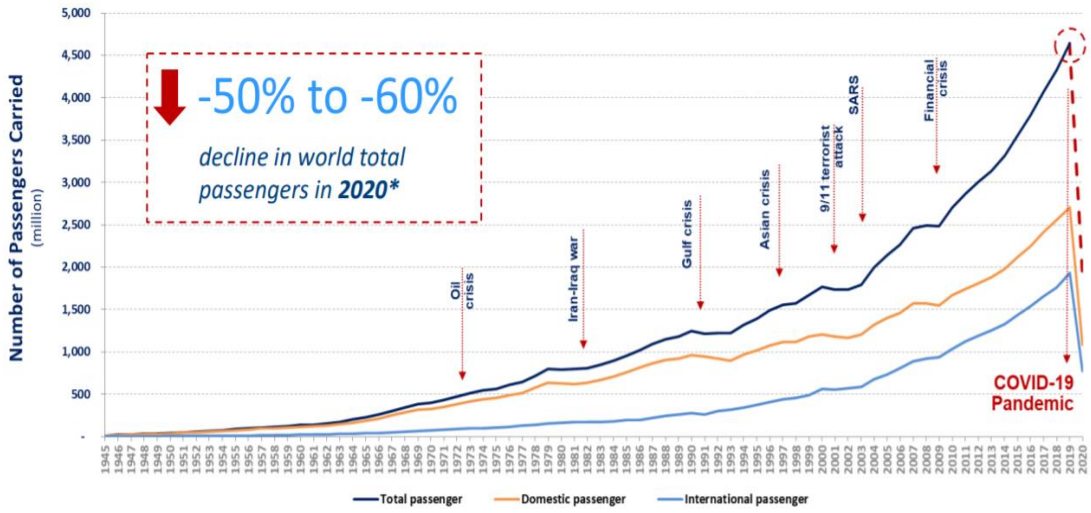


Figure 1.1: World passenger traffic trends from 1945 to 2020 [1].

Besides, the revenues of the largest two companies in the commercial aircraft field in 2019 were 70.5 billion euros and 76.6 billion dollars for Airbus and Boeing, respectively [4], [5]. These numbers underline the substantial positive trends in the aviation sector.

The transportation sector is the largest source of carbon dioxide (CO_2) emissions in the US, accounting for 28% [6]. Considering that the aviation sector is expected to recover from COVID-19, the annual increase in aircraft passengers is estimated to be around 6.4%, while the annual freight traffic growth rate will is 4.2% [7]. This means that with the current aviation transportation technology, CO_2 emissions will continue to increase dramatically. Due to concerns about global warming and pollution, many organizations have set goals to limit pollution in the atmosphere and reduce greenhouse gases, including the National Aeronautics and Space Administration (NASA) and the Advisory Council for Aviation Research and Innovation in Europe (ACARE). NASA and ACARE's environmental goals relative to the year 2000 are shown in Table 1.1 [8]–[10]. As the table shows, the targeted improvements for both NASA N+3 and ACARE 2050 are extremely high, with reductions of CO_2 by 75%, NOx by 90% and external noise by 65%; these targets are unfeasible using traditional aircraft design (turbofan or piston engine) due to the relatively low efficiency of ~ 40% [11]. To achieve these goals, aircraft, including the propulsion system, must work with superior efficiency.

Table 1.1: NASA and ACARE environmental goals [8]–[10].

CATEGORY	ACARE 2020	ACARE 2050	NASA N+2 ~2020	NASA N+3 ~2030
CO_2 reduction	50%	75%	-	-
NO_x reduction	80%	90%	75%	80%
Ex. noise	50%	65%	-42 dB	-71 dB
Fuel burn	50%	-	50%	60%

One of the obvious solutions in achieving environmental goals is using battery banks as the power source in aircraft, similar to electric vehicles. The use of battery banks as a power source is feasible in small size, ultra-light aircraft such as Airbus's E-Fan, Eviation Alice and Harbour Air's seaplanes [12]–[14]. The E-Fan was a two-seat fully electric aircraft powered by a battery-only system, produced by Airbus for pilot training and two-seat touring in 2014 [12], while the Eviation Alice is a nine-passenger battery-only airplane that can fly up to 650 miles [13]. However, it is not currently possible to fly commercial aircraft (>100 passengers) using battery-only systems due to the relatively low energy density of batteries (250-320 Wh/kg) [13], [15].

The turboelectric distributed propulsion (TeDP) system is considered one of the best approaches for future large-scale aircraft to achieve the desired environmental goals. The main idea of the TeDP system is replacing the traditional engine (turbofan) with a turboshaft that runs electric generators connected to electric motors via a direct current (DC) microgrid that includes converters to control motors/propellers to produce the thrust required by the aircraft [16]. This facilitates the hybridization of energy sources and superconducting components to improve system performance [16].

There are several advantages of the TeDP system, including the elimination of alternative current (AC) losses, the lack of a need to synchronize several AC generators as in an AC network, and a decoupling of the propulsion system and engine speeds, thereby improving system efficiency [17], [18]. The propulsion system of the turboelectric aircraft (TeA) needs to produce 30,000 hp for maximum thrust during take-off, meaning that the generation unit needs to produce 22.4 MVA solely for the propulsion system [19]. The airborne DC microgrid has a relatively high power demand, and the DC-link's voltage is in the range of 4 to 10 kVDC [16], [20].

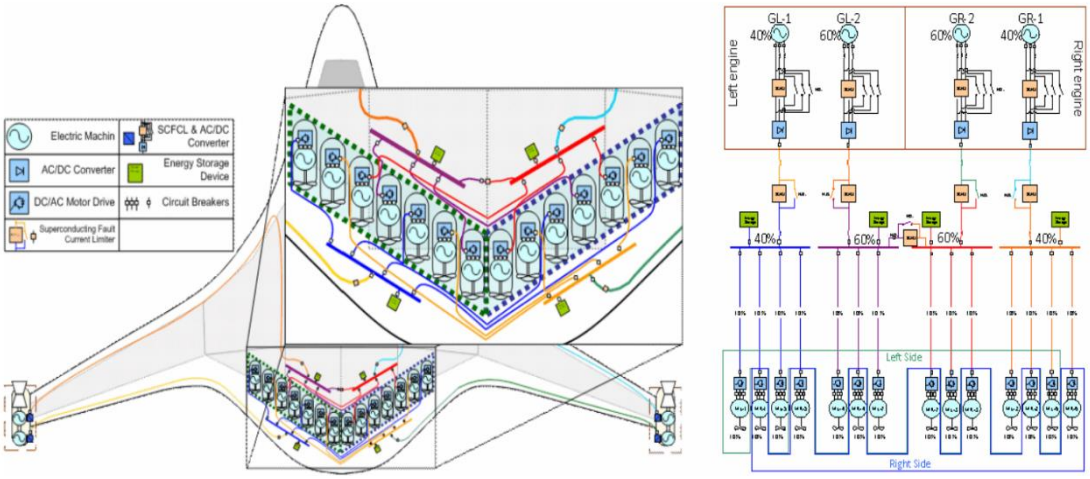


Figure 1.2: Rolls-Royce and NASA's TeDP system architecture concept [16]

The merging of electrical components in aircraft and the installation of onboard electrical power systems offer several design opportunities for optimization and system improvement. However, there are several design challenges for the TeA power system.

Although DC microgrids offer several advantages over AC systems, as mentioned earlier, the protection of DC distribution systems against faults is a significant challenge due to the high magnitude of fault currents and the absence of zero-crossing points [21], [22]. Several factors determine the fault current characteristics, including the DC-link capacitance, line impedance, voltage level, and grounding impedance [23], [24].

This thesis investigates the DC faults in the TeA power system architecture. The fault current is expected to be substantially high due to the compact nature of the electrical network as well as the relatively high voltage level and low line impedance. A key solution to support the protection system in the TeA during fault scenarios is the use of a superconducting fault current limiter (SFCL). SFCL devices have a low impedance during normal operation. However, when a fault occurs, a fast increase in SFCL impedance occurs to mitigate the destructive effects caused by the fault. Due to this behaviour, SFCLs are integrated into the TeA power system to support the CBs

during fault scenarios. In this study, SFCLs with different copper stabilizers and shunt resistors are investigated. Finally, a superconducting magnetic energy storage (SMES) system is integrated into the power system architecture to stabilize the DC link during temporary power losses.

1.2 Research motivations

The motivations for this research mainly stem from three factors:

- The first motivating factor is the environment. According to the US Environmental Protection Agency (EPA), transportation is the largest source of CO_2 in the US, at 28% [6], and CO_2 emissions grew by 2.7 % in 2018 [25]. Environmental concerns have motivated both NASA and ACARE to set goals to achieve a better, cleaner and safer environment for current and future generations. Against this backdrop, aircraft electrification is a promising solution to the pollution caused by traditional aircraft. Fig. 1.3 shows different scenarios for CO_2 emissions until 2050 relative to 2005 levels as predicted by the IATA [26]. With no action, CO_2 emissions will increase dramatically.

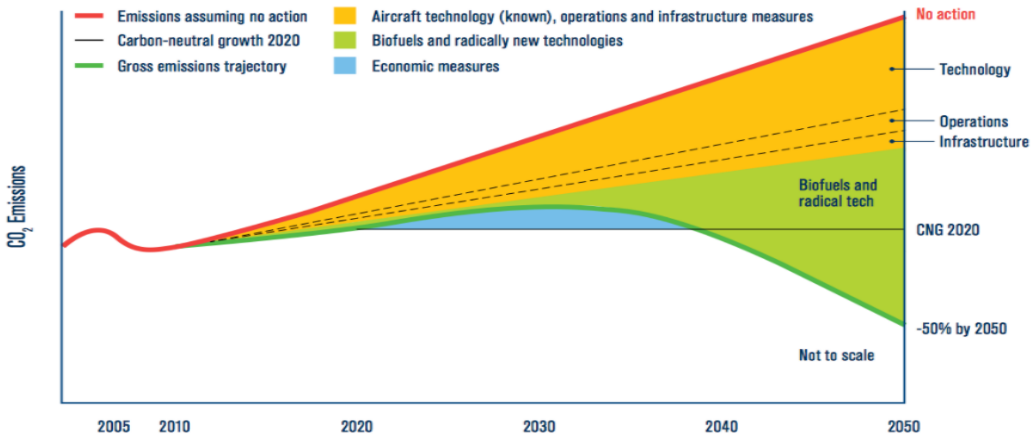


Figure 1.3: Schematic CO2 emissions reduction roadmap [26].

- The second factor is the positive growth in the aviation sector for both large and small-scale aircraft. Excluding the impact of COVID-19, which the aviation sector will eventually overcome, the average annual growth rate for passenger numbers was estimated to be 6.4%, while the growth rate for freight traffic was 4.2% [7]. With the constant growth in the aviation sector, aircraft should work at the highest possible level of efficiency with the best available/feasible technology for both environmental and economic concerns.
- The third factor is the necessity of designing a safe, reliable and resilient electrical network for the TeA. Safety and reliability have always been crucial for electrical networks, more so when the load is sensitive and is related to human safety as in aircraft. DC fault analysis for the medium-voltage DC (MVDC) TeA power system can help in selecting protection equipment and ensure system reliability and a high level of system resilience. The TeA power system architecture is considered a power-dense electrical system, with relatively high voltage levels and low line impedances, which all lead to extremely high fault currents. Conventional methods of reducing fault currents, which include increasing system impedance, have significant operational shortcomings, such as increased system losses, thereby reducing system efficiency. In addition, the fault current rise time in power-dense electrical networks such as those in TeA is shorter than the operational time of available DC CBs (which can take up to 4 msec). The use of SFCLs reduce the fault currents and close the time gap between the fault occurrence and fault clearance, thus minimising/avoiding these issues, consequently improving aircraft reliability and supporting the protection system of the TeA. This thesis starts with the DC fault analysis in the TeA to showcase the extreme behaviour

of the fault currents, which is the basis for planning and building the power protection system. A detailed SFCL model with different stabilizers and shunt resistors is demonstrated to reduce the fault currents. The importance of SFCL in protection systems is demonstrated by integrating them into CBs.

1.3 Principal contributions

The contributions of this thesis can be divided into four main categorises:

- Investigating and analysing the DC faults in power-dense electrical systems such as those in TeA. The TeA power system is a compact network with low line impedance and a relatively high voltage level (4 ~ 10 kVDC) which results in high fault currents. In addition, grounding (earthing) in aircraft is investigated for pole-to-ground faults with two different airframe materials, which are aluminium alloys and carbon fiber reinforced polymer (CFRP).
- Designing and testing a multilayer thermoelectric SFCL model for TeA. The SFCL has been modelled in MATLAB/Simulink environment. The model presented in this thesis considers all superconductor tape layers while determining the electrical and thermal behaviours for each layer, and the current is shared between the layers based on the current divider rule. The focus of the SFCL's design is not only on the fault limiting capability but also on the recovery time under load conditions.
- Integrating the SFCLs into the TeA power system and investigating the impact of the SFCLs on the power system's protection, specifically their impact on the fault clearance performance, system resilience and propulsion system stability.

- A SMES with its control method has been designed, modelled and integrated into the TeA power system to improve its stability. This model considers the SMES's capacity to support the propulsion system during temporary power loss.

1.4 Thesis outline

The rest of the thesis is organised as follows:

Chapter 2 is the literature review chapter, which covers three main topics. It starts with an overview of aircraft technologies, the history of aviation, and existing and future aircraft technologies, including the TeA power system architecture. The second topic is DC networks and DC fault analysis, including pole-to-pole and pole-to-ground faults. It is not possible to show a pole-to-ground fault in TeA without demonstrating the grounding (earthing) in aircraft. Hence, the electrical grounding of aircraft is explained in this section. As SFCLs are used/integrated into TeA power systems to reduce faults, superconductivity is covered in this chapter. The discovery and basic properties of SFCLs are demonstrated, and different types are described.

Chapter 3 describes the TeA power system architecture, including the key components of the system: the generation unit, AC/DC voltage source converter (VSC), electric propulsion system, DC/AC variable frequency drive (VFD), transmission lines, and connectors. The TeA power system is modelled in the MATLAB®/Simulink environment. A typical flight cycle is demonstrated for the TeA to show the performance of the system.

After modelling the TeA power system in MATLAB®/Simulink in Chapter 3, **Chapter 4** investigates the DC fault analysis in the TeA power system. This chapter starts by describing the behaviours/stages for pole-to-pole and pole-to-ground faults.

The modelled TeA power system shows the pole-to-pole fault behaviour at different locations of the TeA for the 6 kVDC voltage level. In addition, the pole-to-ground faults are demonstrated with different airframe materials, including metallic materials and CFRP. The 6 kVDC TeA faults are compared to those in the 9 kVDC TeA to showcase the impact of the voltage level on the fault behaviour.

Based on the results of Chapter 4, **Chapter 5** introduces a novel SFCL model that can be integrated into the TeA power system to reduce the fault current and support the protection system during fault scenarios. The novel SFCL model considers both the electrical and thermal characteristics of the superconductor tape which constructs the SFCL. Also, the model has the flexibility to show the current passing through the superconductor's layers. Moreover, the temperature and recovery time of the SFCL can be shown under load conditions. The impact of different copper stabilisers and shunt resistors is also demonstrated.

Chapter 6 presents a brief review of the fault detection methods and circuit breakers in DC systems, which are the causes of the time gap between the fault occurrence and fault clearance. A case study is presented with a pole-to-pole fault at the feeder line. The case study shows that the SFCL is important not only in reducing the current during the fault but also in maintaining the DC-link voltage and the propulsion system speed at the desired values at healthy feeders, giving CBs extra time to operate safely.

Chapter 7 shows the integration of an SMES device into the DC-link in the TeA power system architecture. The SMES can maintain the DC-link voltage at the desired voltage level during temporary power losses. This chapter also presents a case study whereby the SMES can maintain the DC-link voltage for power losses of up to 3 sec.

Chapter 8 provides the conclusion to this research with a summary of the works in this thesis, limitations and suggestions for future investigations.

Chapter Two

2. Literature Review

2.1 Introduction

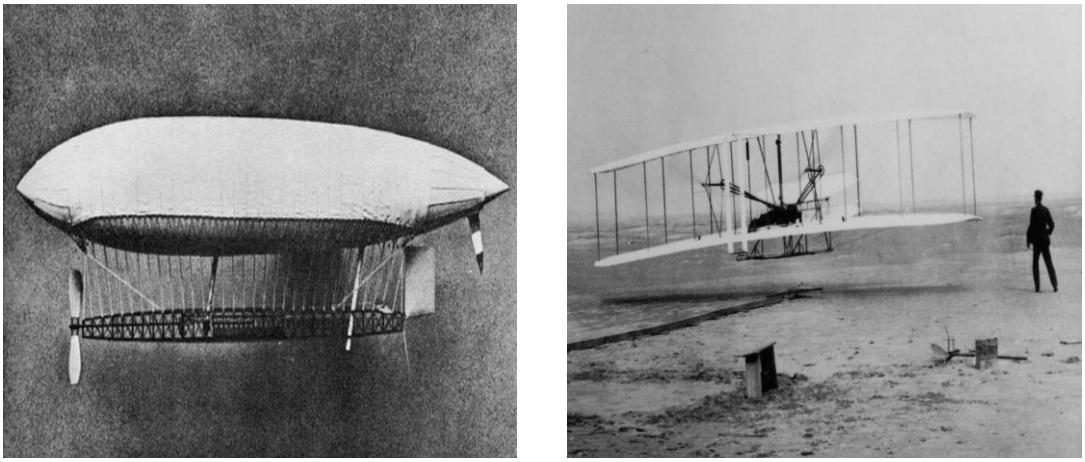
This chapter covers three main topics to achieve the aim of this research. The first topic is an overview of aircraft technologies. It includes the history of aviation, existing and future aircraft technologies, including the TeA power system architecture. The second topic is an introduction to DC power system, including fault analysis and DC circuit breakers. It starts by demonstrating the advantages and disadvantages of the DC microgrids for different applications, including the traditional, electric ships and TeA's airborne DC microgrids. The introduction to fault analysis illustrates the causes and the difference between pole-to-pole and pole-to-ground faults. Furthermore, the electrical grounding in aircraft power systems is outlined. The second topic ends with DC circuit breakers. As the faults are expected to be high in the TeA power system, superconductivity is introduced to exploit SFCL devices to reduce the current during fault scenarios. In addition, SMES is introduced for stability improvement in the TeA's proplusion system; this comprises the third topic.

2.2 Overview of Aircraft Technology

2.2.1 The history of aviation

The dream of flying is one of the oldest human dreams. In the beginning, people tried to imitate birds – without success. The first documented success was in 1884, when two French engineers, Renard and Krebs, built the airship *La France* – a dirigible powered

by a 9 hp electric motor and a 435 kg battery [27], [28]. However, the rise of the internal combustion engine was based on gasoline, setting aside electric propulsion for almost a century [29].



(a) *(b)*

Figure 2.1: (a) La France Airship 1884; (b) Wright brothers' first flight in 1903 [28], [30].

The first heavier-than-air powered flight was carried by the Wright brothers in 1903. Their airplane weight was 341 kg, including the pilot and a 12 hp, 4-cylinder, water-cooled engine [31]. In 1911, Glen Curtiss designed a plane that could take off and land on water, and because it did not need a heavy undercarriage, it could be built larger than any plane had before. Based on the same design, the first scheduled commercial air service began in Florida in 1914, undertaken by Thomas Benoist. The flying boat or seaplane could do the 18-mile trip across Tampa Bay in 23 minutes instead of the two hours it took by boat, and it cost only $5. The flying boat was run by a 75 hp (56 kW) engine and could reach 103 km/h for a range of 200 km [32].

The U.S. government subsequently gained more confidence in the development of planes. Hence, in 1918 Congress approved $100,000 for an experimental airmail service between Washington and New York with an intermediate stop in Philadelphia, to be conducted jointly by the Army and the post office. More routes were added to the mail

services, and by the mid-1920s, the post office mail fleet was flying 2.5 million miles and delivering 14 million letters annually [33].

May 20-21, 1927, is an important date in aviation history. This was when the *Spirit of St. Louis* aircraft, piloted by Charles Lindbergh, made the first nonstop flight across the Atlantic Ocean, from New York to Le Bourget, near Paris. The aircraft was a 223 hp single-engine high wing, and the maximum speed was 200 km/h for a range of 6,600 km [34], [35].

The first modern aircraft was the Boeing 247 in 1933. It was a low-wing, twin-engine, 550 hp military aircraft, able to carry up to 10 passengers at a speed of 189 miles/hour [36]. The DC-3 plane was the first modern plane that enabled airlines to make money carrying passengers in 1936; it had 21 seats with two 1,200 hp engines [37]. The first pressurized cabin was on the B-17 bomber, introduced in 1940 [38]. The pressurized cabin allowed the airplane to fly above 10,000 feet to avoid air turbulence and storms. The first U.S passenger jet was the Boeing 707, which could carry 181 passengers and travel at a speed of 600 miles/hour in 1957 [39]. In 1969, the Boeing 747 was released; it was the first wide-body jet, with two aisles and four engines, accommodating up to 450 passengers [40]. In 1972, Airbus flew its first airplane, the A300B. This was a wide-body, medium-range twin-engine jet accommodating 270 passengers [41]. Fly-by-wire (FBW), considered the first use of electricity in large-scale aircraft, was introduced by Airbus into the A320 series in 1980-1987 [42].

(a) (b)

Figure 2.2: (a) Charles Lindbergh and Spirit of St. Louis 1927; (b) DC-3 Aircraft in 1933 [35],[43].

2.2.2 Existing aircraft technology

The current stage of aircraft technology began in the 1980s. In 1987, the first commercial aircraft to use electrical wire was the A320 by Airbus, and the term "fly by wire" was introduced to the field of aircraft technology [42]. The FBW technology reduces the weight and volume of the aircraft by replacing parts of the hydro-mechanical system with electrical systems. In the FBW system, the hydraulic actuator is controlled by a computer system via a sidestick/yoke from the pilot. However, the hydraulic actuator, in the traditional system, took the input command from the pilot via a yoke to cables and pulleys to control the hydraulic actuator. Generally, the standard voltage levels for the electrical system in the aircraft are 115 V, with a fixed frequency at 400 Hz and 235 VAC with a variable frequency (360 to 800 hertz) for an AC high power load and 28 VDC for a low power load. To understand the current design of aircraft, the Boeing 787 is chosen as an example.

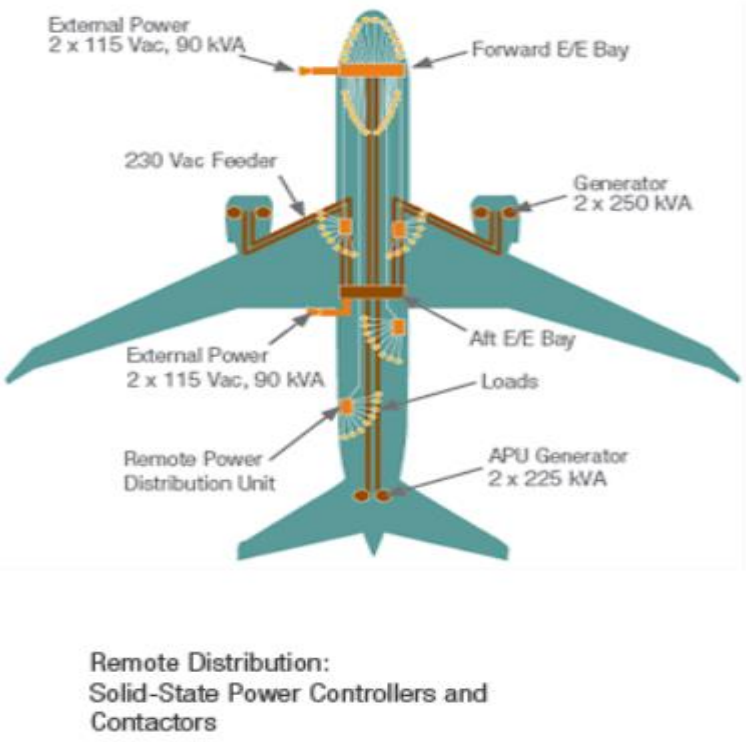


Figure 2.3: Design configuration of the B-787 [44].

The Boeing 787 is considered to have one of the highest power capacities among other aircraft, at 1 MW during a routine flight. It has six generators, two per engine, and two per APU. The capacity of the engine's generators is 250 kVA, the capacity of the APU's generators is 225 kVA, and the voltage level is 235 VAC. The generators are directly connected to the jet engine gearboxes and thus operate at a variable frequency (360 to 800 hertz) proportional to the engine speed. It has four external power sources on the ground with 115 VAC. The forward two are to service the airplane on the ground without running the APU and the rear two are for maintenance activities. The system has two electrical/electronics (E/E) bays. The system has a 28 VDC voltage level for the low load and ±270 VDC for some of the large load, including the cabin pressurization compressor motors, ram air fan motors, nitrogen-generation system compressor used for fuel-tank inerting, and large hydraulic pump motors. Also, there are solid-state power controllers (SSPC) instead of the traditional circuit breaker and

relays for protection. The ±270 VDC system is rectified by four auto-transformer-rectifier units that convert 235 VAC into ±270 VDC [44]. The system has two battery banks, a primary battery, and an APU battery unit. It is a lithium-ion (lithium cobalt oxide) battery with 32 V (8 cells), 150 A, and 28.6 kg [45].

2.2.3 Electric propulsion aircraft

Electric propulsion (EP) is a method of aircraft propulsion that uses electrical power to generate thrust and accelerate the propellers through various electrical means. The main goal of EP is to reduce greenhouse gases and improve aircraft efficiency. NASA's Glenn Research Center has proposed six different electric propulsion architectures, as shown in Fig. 2.4 [46]. The EP architectures can be classified into three main categories: all-electric aircraft (AEA), hybrid electric aircraft (HEA) and TeA. The obvious solution to aircraft electrification is by following the approach used for electric vehicles, i.e. making the entire aircraft electric. AEA has zero emissions and less noise. Currently, there are several AEA operated battery-only systems, including the E-Fan and Alice projects. The E-Fan was a two-seat fully electric aircraft powered by a battery-only system produced by Airbus for pilot training and two-seat touring in 2014 [12], while the Eviation Alice is a nine-passenger battery-only airplane that can fly up to 540 NM (≈ 621 miles). The battery bank of the Alice airplane is a Li-Ion 920 kWh, with a total weight of 3,600 kg, which quantifies for 255.5 Wh/kg energy density. It has three electric motors at 260 kW each [13]. However, while it is possible to fly ultra-light and small-size aircraft with battery-only systems, it is not currently possible to fly commercial aircraft with over 100 passengers using battery-only systems due to the low energy density (kWh/kg) of batteries (250-320 Wh/kg) [13], [15].

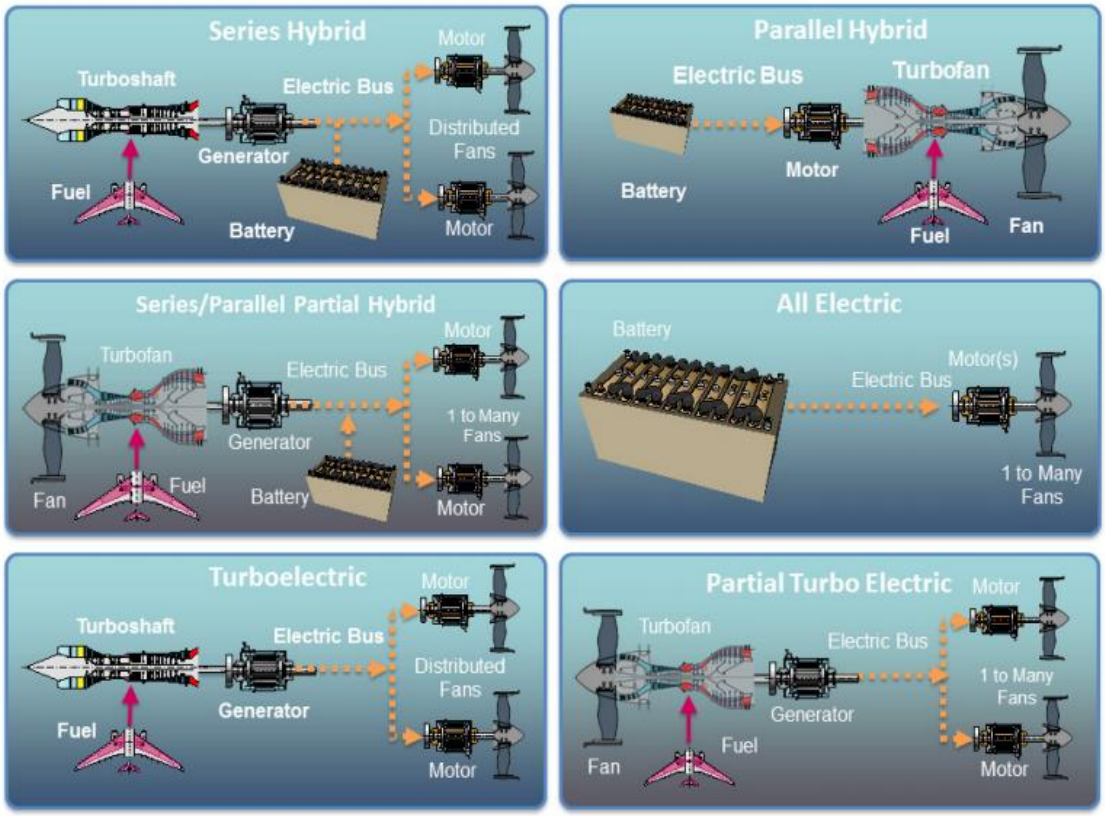


Figure 2.4: Electric propulsion architectures [47].

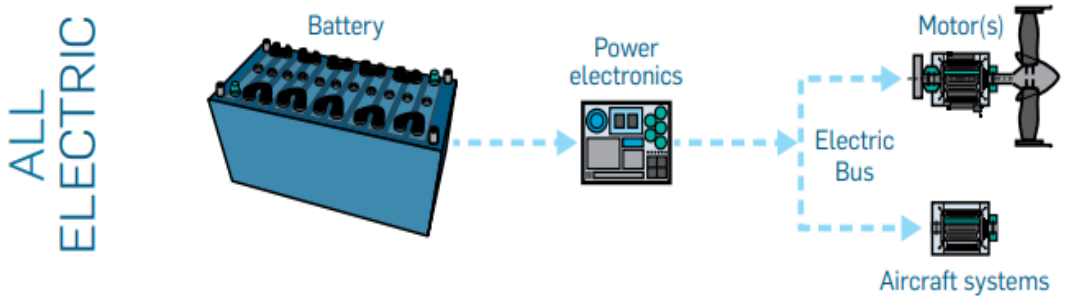


Figure 2.5: All-electric aircraft system architecture [48].

The best example of a HEA is the E-Fan X project. Airbus, Rolls-Royce and Siemens teamed up to launch this hybrid-electric flight demonstrator. Airbus is responsible for the overall system integration. Rolls-Royce is in charge of the turbo-shaft engine, two-megawatt generator, and power electronics. Siemens is in charge of the 2 MW electric motor with its control, including the DC/DC, DC/AC rectifiers and power distribution system. The project is considered an important step to achieving the environmental goals of the European commission's Flightpath 2050 vision for aviation. In this

demonstration project, one of the four jet engines is replaced with a 2 MW electric motor, and the electric propulsion unit is powered by a hybrid generator/battery system. During take-off, both battery and generator supply the electric motor.

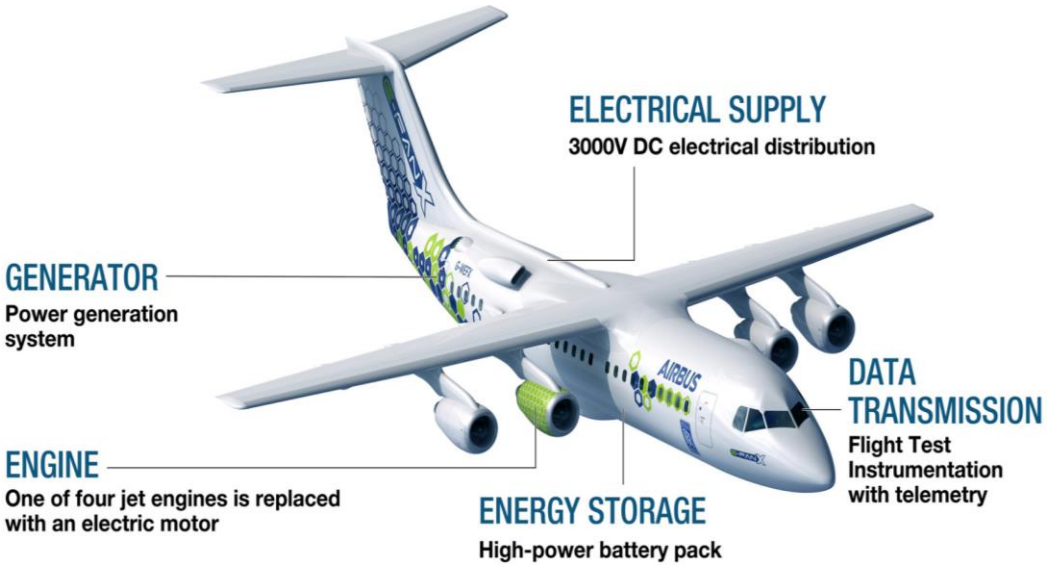


Figure 2.6: Technical specifications of the E-Fan X [49].

The DC-link voltage is 3 kVDC in this project. Fig. 2.6 shows the technical specifications of the E-Fan X, which was expected to fly in 2021 [50]. However, Airbus and Rolls-Royce made a joint decision to bring this project to an end this year (April 2020) for several reasons, including the impact of Covid-19 [51].

When it comes to the TeA, the most notable TeA concept is NASA's N3-X, which was proposed under NASA's Research and Technology for Aerospace Propulsion (RTAPS) initiative [52]. It is a TeDP system with an airborne electrical microgrid. The main idea of the TeDP is to relocate the gas turbine engines away from the propulsors, resulting in the TeA's power system architecture looking like a small microgrid with a number of turboshaft engines and motors connected to fans or propellers, which are controlled by power electronics. Fig. 2.7 shows the power system architecture and Fig. 2.8 presents the complete power system of the TeA baseline architecture.

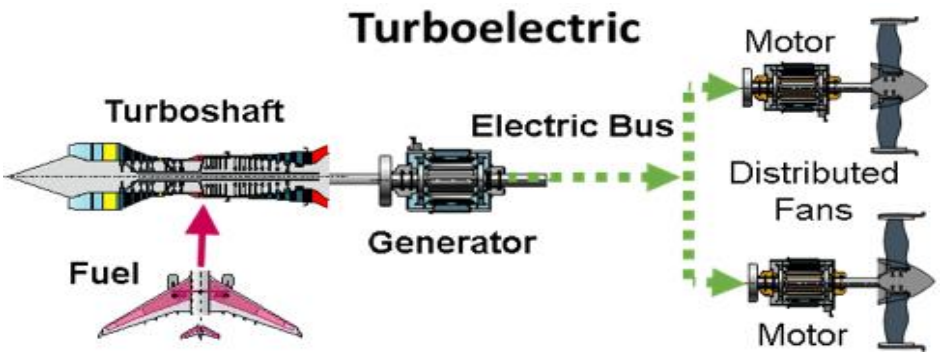


Figure 2.7: Turboelectric aircraft power system architecture [53].

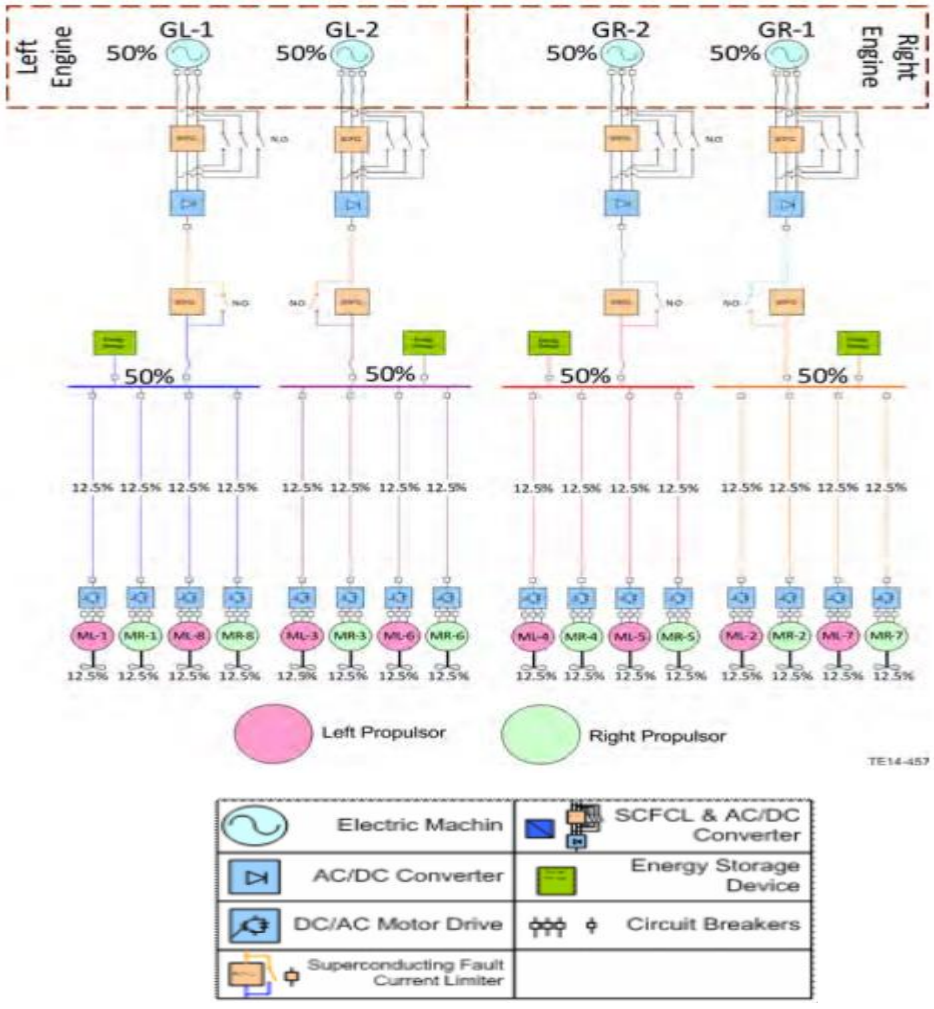


Figure 2.8: Baseline architecture diagram for the turboelectric propulsion system [16].

The baseline architecture consists of two turboshaft engines connected to four electrical generators. Each electrical generator independently supplies one electrical

system. Each electrical system consists of a generator, AC/DC VSC, DC bus line with one energy storage device, and four motors connected to four propellers. The TeA needs at least two electrical systems to operate safely, while each electrical generator provides 50% of the required power and each motor provides 12.5% of the required thrust [16]. The TeA power system architecture is discussed in detail in Chapter 3 because it is chosen as the platform upon which to carry out the DC fault analysis in this study.

2.3 DC power system

DC microgrids have been the center of much focus and research for both academia and industrial institutes over the past few decades. This was led by several factors, including the growth of distributed renewable energy sources, increase in DC loads and the rapid improvement of power electronics [54]. DC microgrids have demonstrated better efficiency, reliability and control simplicity over the AC microgrids [22], [55]. The advantages of DC microgrids over the AC ones attracted several applications, including ships and aircraft.

In electric ships, the onboard DC microgrid uncovers several opportunities for efficiency improvements and weight/space savings. The lack of a need to synchronise all equipment at a specific frequency (usually 60 Hz on ships) is the way to achieve better efficiency in the onboard DC microgrid. Controlling each power device independently opens up various ways of fuel consumption optimization [56]. IEEE released a recommended practice guide for 1 kV to 35 kV MVDC power systems on ships to be used as guidelines for MVDC ship stakeholders and designers to achieve the desired reliability, survivability, and power quality [57].

In aircraft, there are several advantages of the airborne DC microgrids, including the elimination of AC losses, the lack of a need to synchronise several AC generators as in an AC network, and the decoupling of the motor/propeller and engine speeds, thereby improving system efficiency [17], [18]. Two reports from NASA were published in 2015 to give guidance and recommendations for the airborne DC microgrid for TeA power systems [16], [20]. The power system architecture of an airborne DC microgrid for TeA is shown in Fig. 2.8.

Although there are several advantages of the DC microgrid over the AC type, as mentioned earlier, the protection of DC distribution systems against faults is considered to be a significant challenge.

2.3.1 DC fault analysis

Due to the high magnitude of fault currents and the absence of zero-crossing points in DC microgrids, the protection of DC power systems is considered as a real challenge [21], [22]. Several factors determine the fault current characteristics, including the voltage level, DC-link capacitance, line impedance, and grounding impedance [23], [24]. There are mainly two types of DC faults in bipolar systems, namely pole-to-pole faults and pole-to-ground faults. The following two subsections describe the two types of faults.

2.3.1.1 Pole-to-pole fault

Pole-to-pole faults occur when the positive pole is directly connected to the negative pole due to insulation failure or human error. When the positive pole touches the negative pole, a low line impedance is presented. Thus, the system is exposed to a high

fault current, causing severe damage to the electrical system [58]. Fig. 2.9 shows the schematic of a pole-to-pole fault.

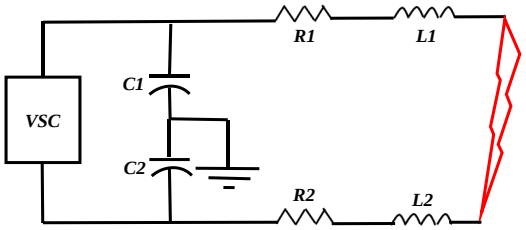


Figure 2.9: Equivalent circuit of a pole-to-pole fault.

2.3.1.2 Pole-to-ground fault

Pole-to-ground faults occur when either the positive or negative pole is connected directly to the ground. This type of fault usually occurs due to insulation degradation. A pole-to-ground fault is more likely to happen, yet it is not as dangerous as the pole-to-pole fault [58], [59]. Because the ground has a significant impact on the fault in the pole-to-ground fault, grounding in aircraft is discussed in the next section. Fig. 2.10 shows the schematic of a pole-to-ground fault.

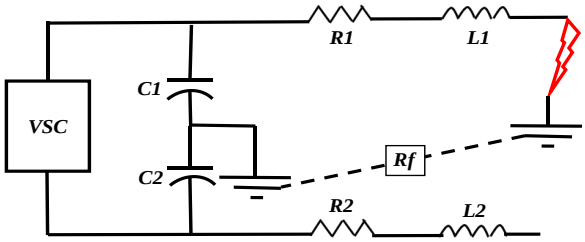


Figure 2.10: Equivalent circuit of a pole-to-ground fault

2.3.1.2.1 Grounding in aircraft

Grounding is a necessity in all electrical systems, mainly to protect equipment and human lives (operators and users alike) as well as to facilitate fault detection. This is done by providing an alternate path for the significant flow of current within a system when a fault occurs. In traditional networks, the ground path is provided by connecting

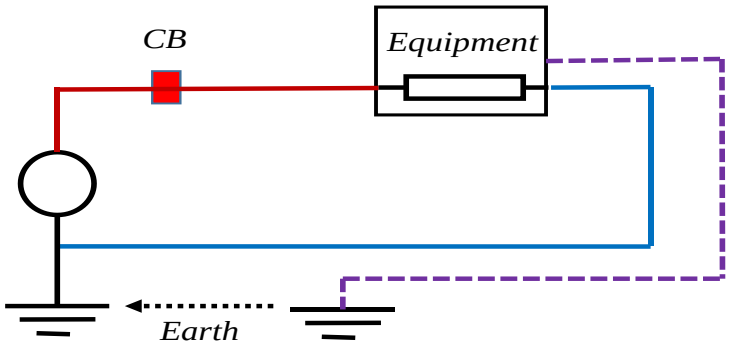


Figure 2.11: Grounding system in a traditional electrical network.

the metallic part of the equipment to the earth, making a high-voltage discharge path available when the internal insulation of the equipment fails for any reason, as shown in Fig. 2. 11. If the equipment is not appropriately grounded/earthed, direct contact with it will result in permanent damage, if not lethal electric shocks [60], [61]. However, in relation to aircraft cruising at altitudes reaching 30,000 feet, a direct connection to the earth is not a feasible option. Thus, the airframe (fuselage) is used for grounding instead.

In the past, the airframe was made of aluminium alloys, as shown in Fig. 2. 12(a), which can be used as grounding, bonding, voltage reference and a current return path due to their high electrical conductivity, thereby reducing the number of wires onboard the aircraft by half [62]. However, the evolution of CFRP, which have a better weight-to-strength ratio, has re-shaped the aircraft fuselage of aircraft, such as the Airbus A350 and the Boeing 787. Because the electrical conductivity of CFRP is very low compared to aluminum, it cannot be used as a current return path. Instead, there are two metallic networks to ensure the low resistivity of the airframe: an electrical structure network (ESN) implemented in the fuselage, and a metallic bonding network (MBN) in the non-pressurized zones (wings, fin and tails). These work together to ensure the low resistance of the airframe and allow it to act as grounding, bonding, and voltage reference and personal protection, as shown in Fig. 2. 12 (b) [63]–[65].

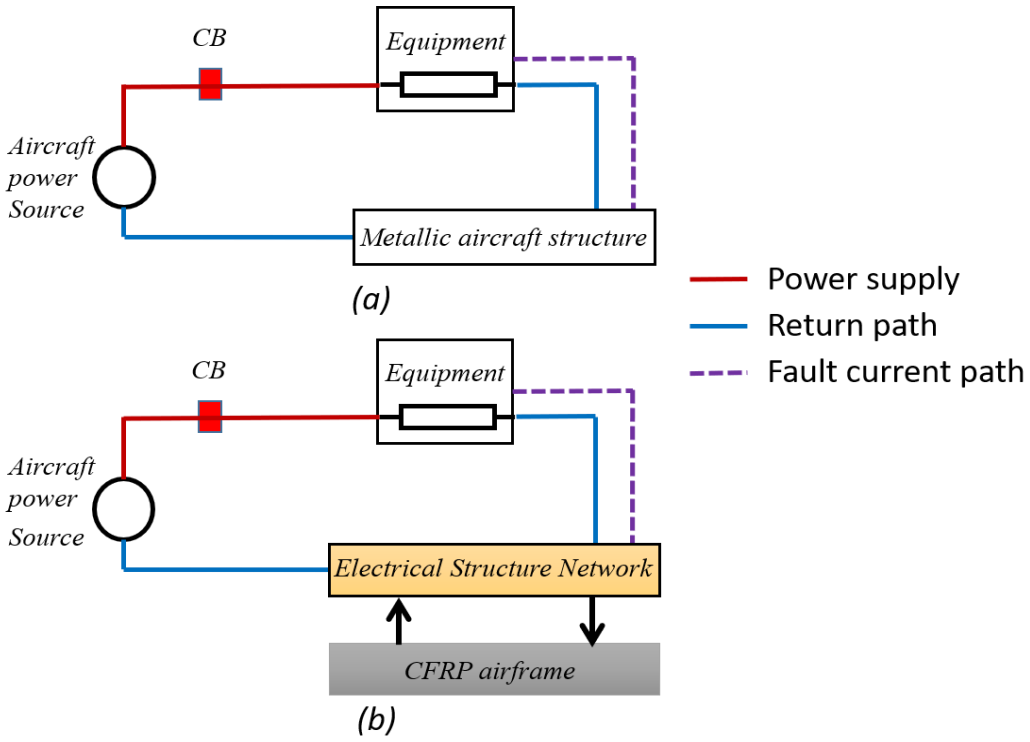


Figure 2.12: Grounding system of different electrical networks; (a) metallic aircraft and (b) CFRP aircraft.

2.3.2 DC circuit breakers

The distribution network in the TeA is considered an MVDC power system with 6 kVDC rated voltage. There are several advantages to using an MVDC network, as mentioned earlier, including the elimination of AC losses, the lack of a need to synchronize several AC generators as in AC networks, and the decoupling of the propulsion system and engine speeds, thus improving system efficiency [17], [18]. However, there are several challenges, including the circuit-breaking in MVDC systems. Because of the natural absence of zero-crossing in the current waveform, DC current-breaking is much more challenging than in AC systems. The DC circuit breakers can be divided into three main types, namely mechanical DC circuit breakers, solid-state DC circuit breakers and hybrid DC circuit breakers [66].

2.3.2.1 Mechanical DC circuit breakers

The topology of the mechanical DC circuit breaker (resonance DC circuit breaker) is shown in Fig. 2.13. The resonance CB consists of three parallel paths: the normal current path where the mechanical switch is located, the current commutation path, which consists of the capacitive and inductive elements, and the energy dissipation path, which consists of the surge arrestor, metal-oxide varistor (MOV). During normal operation, current flows through the normal current path. However, when a fault occurs, the mechanical switch receives an interrupting command, and the mechanical switch opens. As a result, an arc will occur, which redirects current to the current commutation path. In this stage, the current oscillations are exponentially increased by the inductive and capacitive elements to generate the zero-crossing point. When the oscillation can completely oppose the normal path current, the arc is extinguished. Finally, current flows to the energy dissipation path to absorb the residual energy in the system. The mechanical CBs have low contact resistance during normal operation. However, their interruption time is relatively long, in the range of ten milliseconds, due to the need for zero-crossing point generation [66], [67].

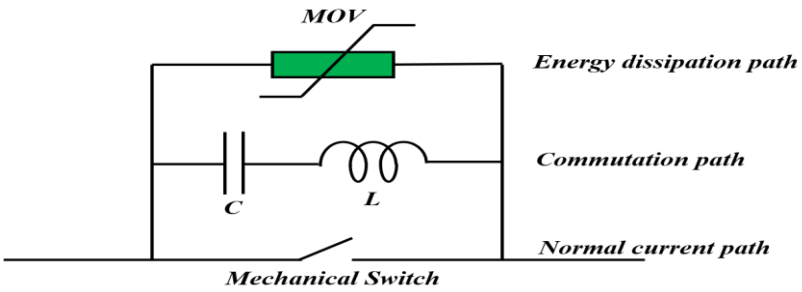


Figure 2.13: DC mechanical circuit breaker topology.

2.3.2.2 Solid-state DC circuit breakers

The solid-state circuit breaker topology relies solely on semiconductor devices, such as IGBTs or GTOs. During normal operation, current flows through the solid-state devices

and when a fault occurs, the solid-state switches turn off and block the current. A parallel MOV device is used to absorb and dissipate the stored energy in the system inductance and limit the voltage across the semiconductor devices. Solid-state DC circuit breakers can interrupt a fault within 100 µsec [67]. However, the high on-state losses of the solid-state switches compared to mechanical and hybrid breakers are the major drawback of solid-state circuit breakers [68]. The IGBT-based solid-state DC circuit breaker topology is shown in Fig. 2.14.

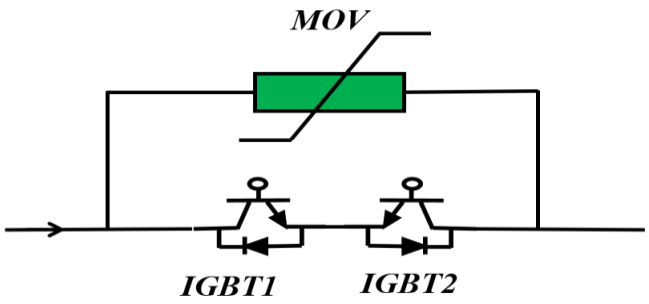


Figure 2.14: Solid-state DC circuit breaker topology

2.3.2.3 Hybrid DC circuit breakers

A hybrid circuit breaker topology consists of the two types of switches, namely mechanical switches and semiconductor switches. During normal operation, current flows through the mechanical switch, which has low on-state resistance. When a fault is detected, the mechanical switch is open and the current is commutated to the semiconductor switches branch by the arc voltage of the mechanical switch. The semiconductor switches conduct the current until the mechanical switch is entirely open. At this stage, the semiconductor switches are turned off and the MOV starts to conduct, absorb and dissipate the stored energy in the system and the fault is cleared. The hybrid circuit breaker topology is shown in Fig. 2.15.

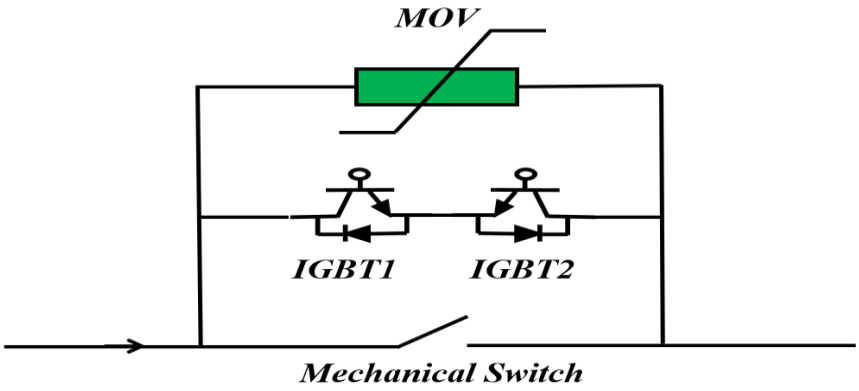


Figure 2.15: Conventional hybrid circuit breaker topology.

The hybrid circuit breaker has lower losses than the solid-state circuit breaker as well as faster operation compared with the mechanical circuit breaker as it has a solid-state branch [67]. In conventional hybrid DC circuit breakers, the commutation of the current from the mechanical switch to the semiconductor branch relies solely on the arc voltage. If the arc voltage is not high enough, the mechanical switch may fail to open.

There have been several improved topologies based on hybrid DC circuit breakers to aid the commutation and to improve the operation time. One of the best examples of these is the proactive hybrid DC circuit breaker, which was proposed and developed by ABB, as shown in Fig. 2.16.

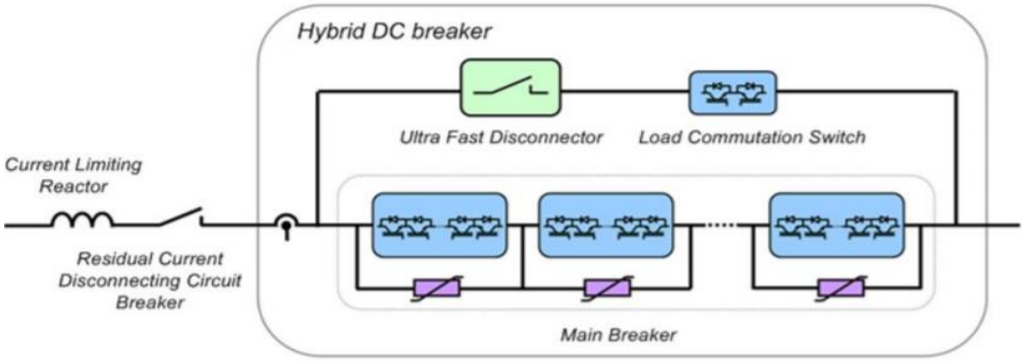


Figure 2.16: Proactive hybrid circuit breaker [69].

The proactive hybrid DC circuit breaker topology has three parallel paths; during normal operation, current flows through an ultra-fast disconnector (UFD) and a load commutation switch (LCS) in series. The LCS has sufficient solid-state switches to commutate the current to the main breaker path when a fault occurs. The sequences of the hybrid DC circuit breakers are as follows: when a fault occurs, the hybrid DC circuit breaker receives an interruption command, and the LCS opens to commutate the current to the main breaker path, allowing the UFD to open. The UFD is a mechanical switch, which is used to isolate the LCS from the primary voltage across the mainline. After that, the solid-state switches, in the main breaker path, open and block the current. The parallel MOV devices are used to absorb and dissipate the stored energy in the system inductance and to limit the voltage across the semiconductor devices. The proactive hybrid DC circuit breaker of ABB can clear a fault in 5 msec [69]. Several hybrid DC circuit breakers have been proposed and simulated/developed, including hybrid DC circuit breakers with a commutation booster [70], [71], superconducting hybrid DC circuit breakers [72], and hybrid DC circuit breaker with a coupled inductor [73]. A prototype of the hybrid DC circuit breaker with a coupled inductor connected in series is capable of interrupting 200 A DC current within 4 msec [73].

2.4 Superconductivity

2.4.1 Discovery

In 1911, superconductivity was discovered by Prof. Heike Kamerlingh Onnes at Leiden University. The resistivity of mercury disappeared when he cooled it to the temperature of liquid helium, i.e. 4.2 K (-269℃). This phenomenon was defined as superconductivity, and he received a Nobel prize for this discovery in 1913 [74].

Since then, many superconducting materials have been discovered, such as lead, tin, niobium-titanium (Nb-Ti) and niobium-tin (Nb3Sn), which are all considered low-temperature superconductors (LTS), $Tc < 30$ K. The applications for superconductivity were limited in the first 60 years because of the extremely low temperature needed for them to work in a superconducting state. In addition, the superconductivity state can be easily destroyed with a relatively small magnetic field and small current. Therefore, superconductivity was only attractive for research and study, and not so much for use in technology [75].

The first discovery of high-temperature superconductors (HTS), at $Tc > 30$, was in 1986, when J. George Bednorz and K. Alex Müller discovered that the transition temperature of a lanthanum-based cuprate perovskite material is 35 K. Shortly after that, in 1987, a research team at the University of Alabama-Huntsville achieved $Tc > 92$ by substituting yttrium for lanthanum in the Müller and Bednorz molecule, which is known today as yttrium barium copper oxide (YBCO). This discovery opened the door for a cheaper cooling system based on liquid nitrogen (LN_2) at 77 K [76], [77]. Researchers and scientists are still trying to discover more superconductors that can be used at higher temperatures, thereby reducing the costs and challenges of the cryogenic system.

There are several common superconductors, including Nb-Ti and Nb3Sn, which are considered as LTS and are used in MRI devices [78]. On the other hand, common HTSs include bismuth strontium calcium copper oxide (BSCCO) and YBCO, which can be cooled by a cheaper coolant, i.e. liquid nitrogen LN_2 at 77 K.

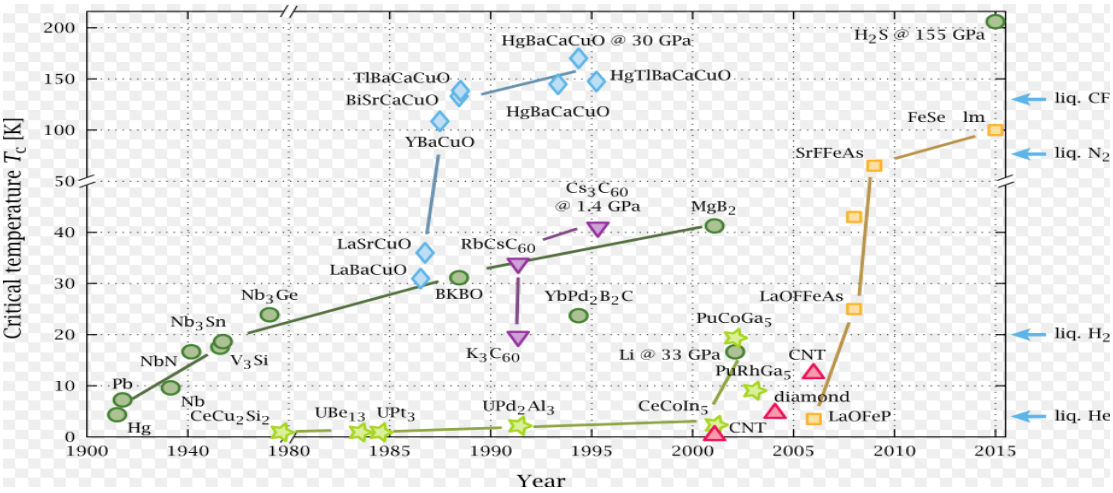


Figure 2.17: The timeline of discovery for superconducting materials [79].

2.4.2 Basic properties of superconductivity

Three inter-related critical elements have to be satisfied in order for a superconductor to work in its superconducting state. The temperature of the superconductor *T* must be less than its critical temperature *Tc*. The applied current density in a superconductor *J* must be less than its critical current density *Jc*. Also, the magnetic field *H* must be less than the critical magnetic field *Hc* of the superconductor.

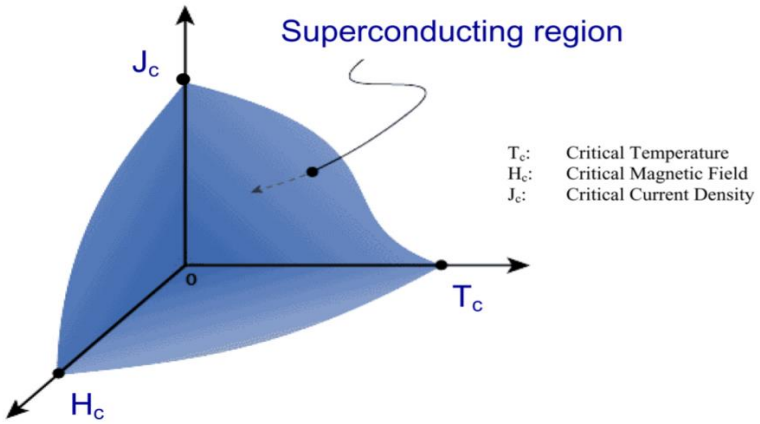


Figure 2.18: The critical superconductivity boundaries [80].

When a superconductor satisfies the superconducting state conditions, the resistance of the superconductor is almost zero. However, if one of the critical values is exceeded, the superconductor will transit from the superconducting state to the normal state, as illustrated in Fig. 2.18.

2.4.2.1 Zero DC resistance

One of the basic properties of a superconductor is its zero electrical resistance when in the superconducting state. This is considered a significant advantage of superconducting cables compared to conventional cables, such as copper and aluminium cables. With the zero-resistance property, small, light superconducting cables can replace large, heavy conventional cables, as shown in Fig. 2.19.

Figure 2.19: Comparison between the size of 12.5 kA conventional cable and superconducting cable [CERN-Cables]

2.4.2.2 Superconducting phase transition

The superconducting materials work mainly in two different states: the superconducting state and the normal state. The characteristics of superconductivity appear when the temperature *T* is below the critical temperature *Tc* of the materials. The value of the critical temperature differs from one material to another. Fig. 2.20 shows the difference between the behaviours of a superconductor and a non-superconductive-metal w.r.t temperature.

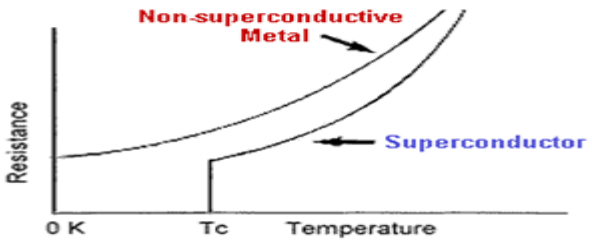


Figure 2.20: The relation between resistance and temperature for a normal conductor and superconductor [81].

2.4.2.3 The Meissner effect

The Meissner effect was discovered in 1933 by German physicists Walther Meissner and Robert Ochsenfeld. They noticed that superconducting tin and lead samples cancelled nearly all interior magnetic fields below a critical temperature. Fig. 2.21 (a) illustrates this phenomenon, and Fig. 2.21 (b) shows the Shanghai Maglev Train, which works using this principle.

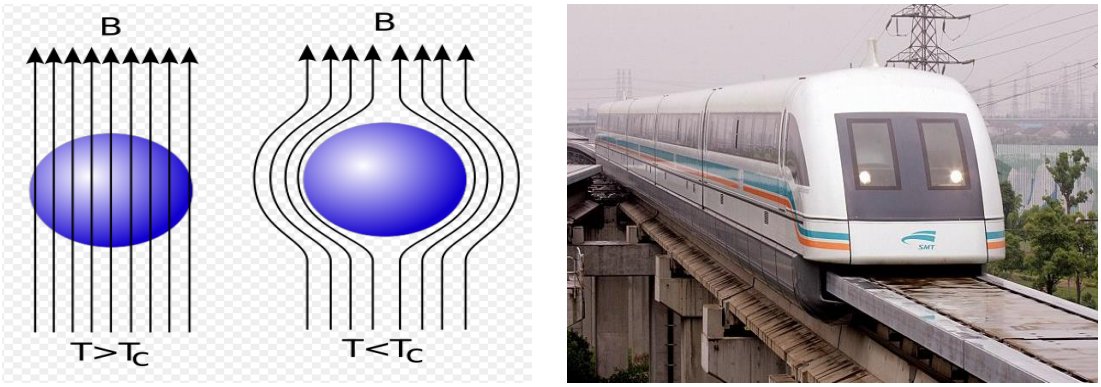


Figure 2.21: (a) The Meissner effect (b) the Shanghai maglev train [82].

2.4.3 Type I and Type II superconductors

Three different factors can destroy a superconducting state: an increase in either temperature, current density, or the applied magnetic field, as shown in Fig. 2.15. From the applied magnetic field perspective, superconductors are classified into two types: Type I, which has minimal value for the critical field *Hc*, such as with mercury (41 mT) [83], and Type II, which has a high value for the critical field *Hc*, such as with YBCO at 140 T. The mercury transits from a superconducting state to a normal state if exposed to a magnetic field above 41 mT. Table 2.1 gives some examples of Type I superconductors' critical fields and temperature values.

Table 2.1: The critical temperatures Tc and critical magnetic fields Hc of Type I superconducting materials [83].

MATERIALS	T_C (K)	H_C (mT)
Aluminium	1.2	10
Lead	7.2	80
Mercury	4.2	41
Tin	3.7	31
Titanium	0.40	5.6

Type II superconductors are capable of working in a high magnetic field. There are two critical magnetic fields: an upper critical field H_{c2} and a lower critical field H_{c1}. If the magnetic field is lower than H_{c1}, Type II superconductors work in the superconducting state. However, if the magnetic field is over H_{c2}, Type II superconductors work in the normal state. The mix-state occurs when the magnetic field is lower than H_{c2} and above H_{c1}. The superconductor works in the superconducting state as long as the vertices are pinned inside the superconductors. Type II superconductors are usually made of metal alloys or complex oxide ceramics. All high-temperature superconductors are Type II superconductors, including BSCCO and YBCO. The upper critical field limits for Type II superconductors are high, such as 140 T for YBCO [84]. Table 2.2 gives some examples of Type II superconductors' critical temperatures and field values [85]. Fig. 2.22 (a) and Fig. 2.22 (b) show Type I and Type II superconductors in the three different states, respectively [86].

Table 2.2: The critical temperatures Tc and critical magnetic fields Hc of Type II superconducting materials [87].

MATERIALS	*TC (K)*	*HC (T)*
NbZr	11	8.3
NbGe	23.6	37
NbAl	19.1	29.5
MgB2	39	32
YBaCuO	93	140
BiSrCaCuO	92	107

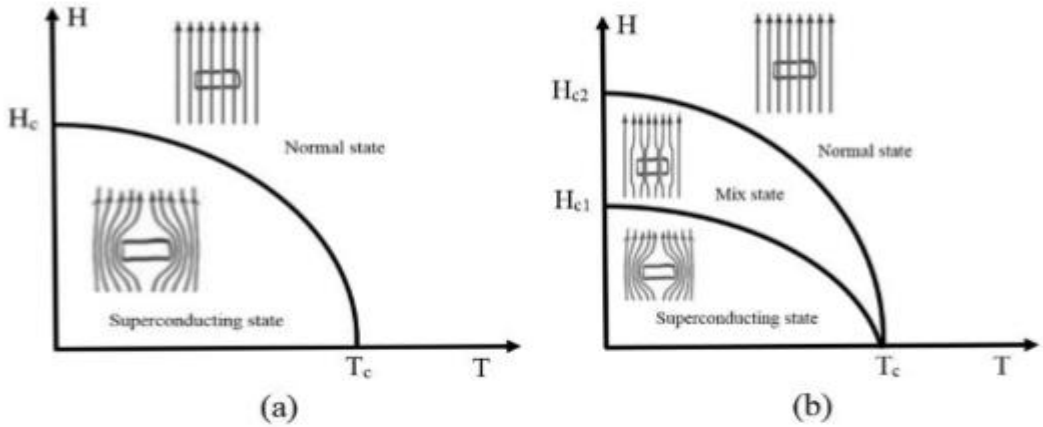


Figure 2.22: The magnetic field of (a) Type I and (b) Type II superconductors [86].

2.4.4 Superconducting fault current limiter (SFCL)

The traditional practice to reduce fault currents in power systems comprises splitting them into subgrids and splitting the busbars, adding a high impedance transformer, or using a current-limiting reactor. However, these methods lead to a permanent increase in the impedance system, which increases the system losses and, therefore, reduces the system efficiency in nominal operation [88]. Another practice is the use of explosive devices like fuses which offer such a function. However, fuses need to be replaced after each trigger, which affects system operation and recovery time. In addition, fuses are

limited to medium voltage levels [88], [89]. These issues raise the need for better performing FCLs. The ideal requirements of FCLs are as follows [89], [90]:

- Automatic trigging and quick, effective fault current limiting capability.
- Low impedance during normal operation.
- Automatic and fast recovery after fault clearance.
- Fail-safe operation mechanism.
- Small size, weight and volume for aerospace applications.
- Cost-effective.

FCLs can be classified into two main types, namely superconducting FCLs and non-superconducting FCLs. Because most non-superconducting FCLs, including solid-state FCLs, suffer from losses in normal operation [91], the focus of this thesis is on the SFCLs. SFCLs are also classified into several types, including resistive-type, shielded iron-core type, saturated iron-core type and bridge-type SFCLs.

2.4.4.1 Resistive-type SFCL

Pure resistive SFCLs (r-SFCLs) have compact and simple designs. Fig. 2.23 shows the schematic diagram of an r-SFCL. During normal operation, current passes through the superconductor branch (superconducting coils) with negligible resistance. When a fault occurs, the current increases rapidly, and when the current exceeds the critical current of the superconducting coils, the superconducting coils quench and develop resistance, limiting the fault current levels. During the quenching process, some of the fault currents are redirected to the parallel impedance, which helps with the fault current

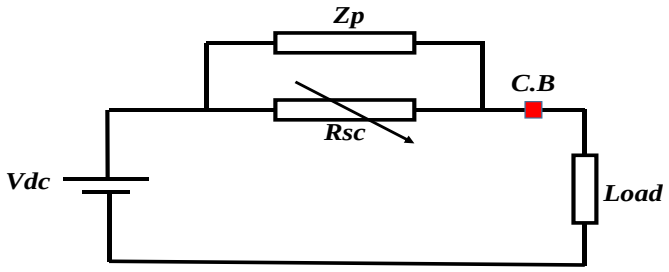


Figure 2.23: Electric circuit of a resistive SFCL with parallel impedance

limiting capability of the r-SFCLs and protects the superconductor coils from overcurrent by providing an alternative path. In addition, the overvoltage, which can appear if the resistance of the superconductor coils increases extremely quickly after a fault occurs, can be avoided by the parallel impedance. The number of coils connected in parallel determines the critical current of the r-SFCLs, and the length of each coil determines its impedance [92].

2.4.4.2 Shielded iron-core type SFCL

Three main elements structure a shielded iron-core SFCL: an iron core, a primary winding by a normal conductor (e.g. copper), and a secondary winding made of a superconducting cylinder which is short-circuited, as shown in Fig. 2.24. During normal operation, the induced current in the superconducting cylinder is less than the critical current. Therefore, the superconducting cylinder acts as a magnetic shielding for the primary winding. In this case, the flux in the iron core is negligible. When the induced current in the superconducting cylinder exceeds the critical value, the cylinder starts to increase its resistivity. The flux starts to penetrate the iron core and impedance is developed on the primary side, which helps to reduce the fault current. This topology suffers from the large iron core and the presence of non-uniform quench for a superconducting cylinder [90], [93].

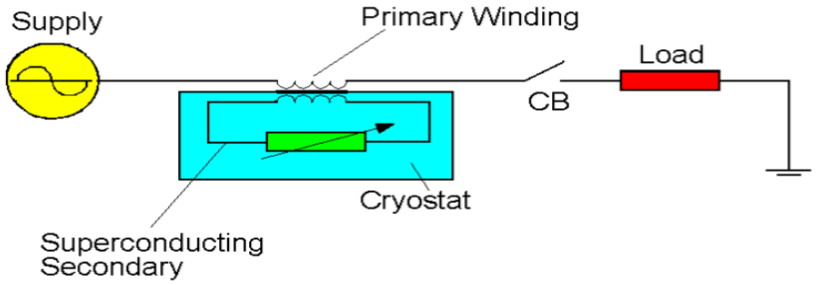


Figure 2.24: Shielded iron-core SFCL concept [94].

2.4.4.3 Saturated iron-core type SFCL

Unlike resistive and shielded iron-core SFCLs, the saturated iron-core SFCL is a non-quenching SFCL. Saturated iron-core SFCLs consist of two iron cores, which are saturated by a DC bias source. Two coils are wound around the two cores to carry the operating current. Other coils are wound around the two cores to saturate them by superconductor tapes connected to the DC bias source, as shown in Fig. 2.25. Because the DC bias source current is much higher than the normal operating current, the iron cores are completely saturated. Therefore, the inductances of the two coils are small during normal operation. When a fault occurs, the operating current *(i_{ac})* increases and forces one of the iron cores, depending on the fault current direction, out of the saturation state, which leads to an increase in the impedance, thereby limiting the fault current levels. The two main disadvantages of saturated iron-core SFCLs are the need for bulky iron cores similar to the shielded iron-core SFCLs. Besides, the DC circuit might be damaged during the fault by an overvoltage, which can be induced in the DC coils. Saturated iron-core SFCLs have several advantages, including fail-safe operation and fast recovery time [95], [96].

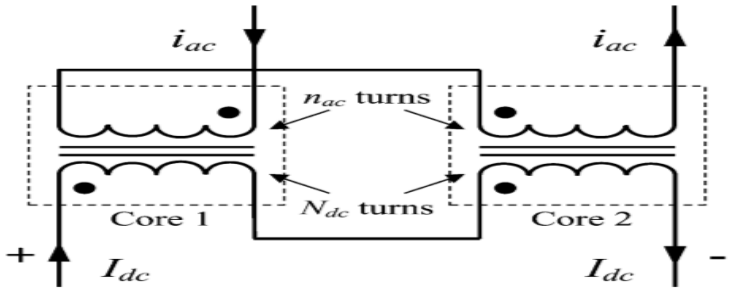


Figure 2.25: Saturated iron-core type SFCL schematic [95].

2.4.4.4 Bridge-type SFCL

The bridge-type SFCL is considered a non-quenching SFCL. The bridge SFCL consists of a superconducting coil, voltage source, and four diodes/thyristors arranged as a full bridge, as shown in Fig. 2.26. During normal operation, the amplitude of the DC current is higher than that of the system AC current and all the diodes are operating in the conducting region. Therefore, the AC current bypasses the inductance with low impedance. When a fault occurs, the operating current (AC current) exceeds the voltage source current (the DC current) in the positive or negative half cycle; hence, a pair of diodes, D1 and D4 or D2 and D3, are turned off, and the superconducting coil inductance limits the fault current. The two main advantages of the bridge-type SFCL are the lack of a recovery time as it is not a quenching SFCL, and the fast fault current limiting capability (within the first half cycle) if thyristors are used instead of diodes. However, because the bridge-type SFCL depends on power electronic switches, it is not fail-safe [97], [98].

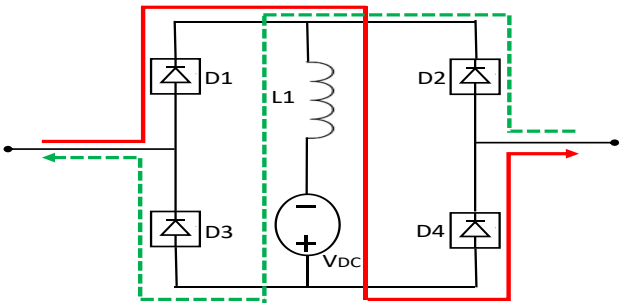


Figure 2.26: Bridge-type SFCL schematic.

2.4.4.4 Applications of SFCLs in power systems

SFCLs can be employed in any part of power system networks, including transmission lines, distribution systems and power stations. SFCLs can also be an essential part of power-dense isolated electrical networks, such as those in electric ships and electric aircraft [99]. The main duties of SFCLs are to limit the fault current during fault scenarios, supporting the protection system to allow CBs to operate safely. In addition, SFCLs are used to secure smooth coupling between subgrids and coupling between busbars. SFCLs are used to connect different generators' feeders or couple dispersed generators. SFCLs can be used in power stations when the power rating is expanded by adding generation units instead of upgrading existing CBs [100]. Currently, the two most common SFCLs in the field are resistive SFCLs and inductive saturated iron-core SFCLs [101], [90]. Some SFCL projects and their specifications are listed in Table 2.3 [102], [103].

Table 2.3: SFCL projects around the world [102], [103], [104], [105], [106].

LEAD COMPANY	COU./YEAR	SFCL TYPE	SIZE
Southern Power Grid	China/2019	Resistive	160kV/1kA
IEE CAS*	China/2019	Resistive	12kV/2.4kA
JZT & BJU**	China/2018	Resistive	220kV/1.5kA
Siemens	Germany/2016	Resistive	10kV/815A
RSE	Italy/2016	Resistive	9kV/15.6MVA
Nexans	UK/2016	Resistive	12 kV/1050A
Nexans	UK/2015	Resistive	12 kV/1600A
Nexans/AmpaCity	Germany/2014	Resistive	12kV/2.4 kA
Nexans/ECCOFLOW	Spain/2013	Resistive	24 kV/1005 A
Innopower	China/2012	Saturated iron-core	220 kV/300 MVA
Zenergy	USA/2012	Saturated iron-core	138 kV/1.3 kA
Nexans	UK/2012	Resistive	12 kV

* The Institute of Electrical Engineering, Chinese Academy of Sciences (IEE CAS).

** Jiangsu Zhongtian Technology and Beijing Jiaotong University (JZT & BJU).

2.4.5 Superconducting magnetic energy storage (SMES)

Energy storage is one of the most important components in power systems. Different energy storage devices are used to manage the energy balance and improve stability in power grids and electrical applications. These energy storage systems can be categorised into four types: electrochemical devices such as batteries, electrostatic devices such as supercapacitors, electro-mechanical devices such as flywheels and electromagnetic devices such as SMES systems [107], [108]. Two features characterise an energy storage system: energy density and power density. Energy density is the amount of energy stored per unit-weight (Wh/kg), while power density is defined as the amount of power (time rate of energy transfer) per unit-weight (W/kg). Fig. 2.27 compares different energy storages in terms of energy density and power density.

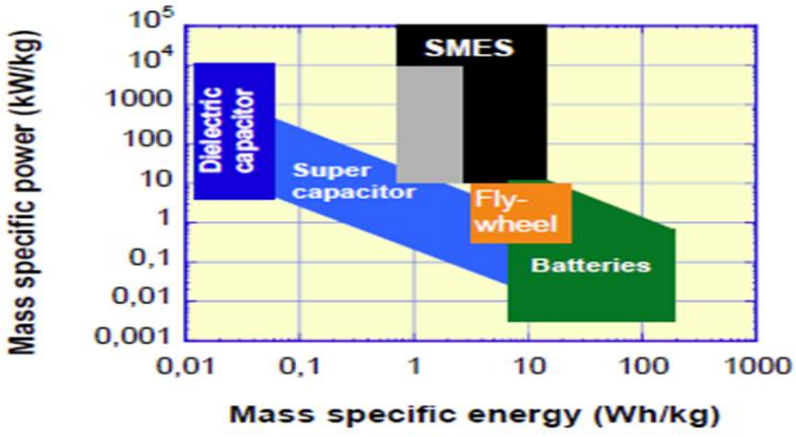


Figure 2.27: Power density vs. energy density for different storage technologies [109].

SMES is an electromagnetic device that stores electrical energy in a magnetic field generated by the flow of a direct current (DC) in the superconducting coil, which is cooled to a temperature below its superconducting critical temperature. The SMES mainly consists of three components, including a superconducting coil, a power conditioning system, and cryogenic refrigerator [110], [111], as shown in Fig. 2.28.

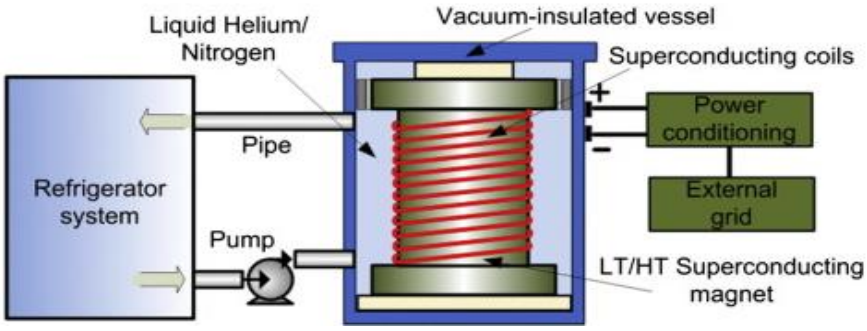


Figure 2.28: Illustration of an SMES system [110].

The basic principle of SMES is that the energy is stored in the magnetic field created by the superconducting coil. Because the superconductor is cooled to below its superconducting temperature, the current will keep flowing in the superconductor even after the voltage source has been disconnected. The stored energy in the SMES can be calculated by multiplying the self-inductance of the coil and the square of the current flowing through it, as shown in Eq. 7.1 [112]:

$$E = \frac{1}{2} LI^2 \tag{2.1}$$

Discharging large amounts of power in short periods of time is the major advantage of SMES, which makes it very well-suited for high-power, short-period applications [111]. Its long lifetime, fast response time and an unlimited number of charge and discharge cycles are considered the main advantages of SMES over other storage systems [113], [114].

The market for energy storage is growing rapidly for many different reasons, including the high penetration of renewable generation in electrical networks, the electrification of transportation, and the use of smart grids. Because SMES has a high power density and fast response time, this makes it a good energy storage option for

some applications in electrical networks [115], [116]. Several studies were performed to take advantage of SMES in different applications. A SMES with a PI controller was proposed to mitigate the effects of renewable energy sources in a microgrid [117]. The use of a hybrid SMES/battery energy storage system based on dynamic droop control was proposed in [118], and another SMES/battery hybrid energy storage system was proposed for use in electric buses, where the storage system was able to adapt to fast changes in the load, hence improving battery lifetime [119]. Table 2.4 shows some of the studied SMES projects, including their scales and applications [110], [111].

Table 2.4: Some SMES Projects [110], [111].

Locations/Organizations	**Technical Data**	**Features/Applications**
Proof principle, tested in a grid in Germany	5 KJ, 2 s to max 100 A at 25 K	World first significant HTS-SMES, by ASC
Nosoo power station in Japan	10 MW	Improve system stability and power quality
Upper Wisconsin by American Transmission	3 MW/0.83 kW h, each 8 MV A	Power quality application reactive power support
Bruker EST in Germany	2 MJ	High temperature superconductors
Korea Electric Power Corporation, Hyundai	3 MJ, 750 kV A	Improving power supply quality for sensitive loads
Chubu Electric Power Co. in Japan	7.3 MJ/5 MW and 1 MJ	Provide comparison to transient voltage
University of Houston, SuperPower & others	20 kW, up to 2 MJ class	UHF-SMES, voltage distribution

2.5 Chapter summary

Because the main goal of this thesis is to investigate DC fault analysis in an isolated power-dense electrical network, such as TeA, and to mitigate the expected extreme behaviour during faults, this chapter covered three topics. First, the platform of this study, which is the aircraft, was outlined. The history of aviation, current technology and some future aircraft were described in section 2.2. The platform of the study is described in detail in Chapter 3. The second topic was an introduction to DC power system architecture and fault analysis. The advantages and the challenges for the DC power system architecture were shown in section 2.3 described. Besides, an introduction to the DC fault analysis for pole-to-pole and pole-to-ground faults, including different ground materials for the airframe was demonstrated in this section. The DC fault analysis is carried out in Chapter 4, with reference to different voltage levels and different grounding materials. Superconductivity was the last topic to be covered in the literature review chapter. The history of superconductivity, basic properties, materials and SFCLs was discussed in section 2.4. Different types of SFCLs were presented in the same section, including the structure and the working principle. In Chapter 5, a resistive SFCL is modelled and tested with different stabilizers, shunt resistors and in different locations in a TeA power system.

Chapter Three

3. Turboelectric Aircraft Power System Description and Modelling in MATLAB®/Simulink Environment

3.1 Introduction

This chapter describes the platform used to carry out the DC fault analysis for the TeA. One generator, one AC/DC voltage source converter (VSC), transmission lines/connectors, and four motors and their variable frequency drives (VFDs) are described and modelled in this chapter. A typical flight cycle with different flight stages, i.e. taxi, take-off, top of climb, cruise, top of descent and landing based on the modelled system is shown to demonstrate the performance of the system's components. The power demand, voltage, current and motor speeds are observed.

In order to carry out the fault analysis of a TeA power system in Chapter 4, one set of the TeA power system architecture, namely the baseline architecture power system, as shown in Fig. 2.8 and proposed by NASA [16], is chosen as the platform to carry out this analysis. Fig. 3.1 is described and modelled in MATLAB/Simulink Simscape block library in this chapter. MATLAB® is a programming platform for engineers and scientists based on the MATLAB® language, with which the most natural computational mathematics expressions can be done using a matrix-based language [120]. Simulink is a block diagram environment for system-level design integrated with MATLAB®. It uses multidomain simulation and model-based design and supports automatic code generation and the continuous testing and verification of embedded systems [121]. The Simscape block library contains several elements and building blocks, including electrical, mechanical and magnetic building blocks [122].

3.2 System and key components description

The TeA power system, a baseline architecture proposed by NASA [16], was chosen to be the platform to perform a typical flight cycle and carry out the fault analysis. In baseline architecture, four generators supply sixteen motors connected to propellers through a DC power system architecture, as shown in Fig. 2.8. The design parameters of the system are shown in Table 3.1.

The ratings of the generators, motors and converters are based on the aircraft data proposed by NASA [16]. The propulsion system needs to produce 22.4 MW for maximum thrust during take-off [19]. Because each motor can produce up to 2.80 MW thrust, at least 8 motors are required to work at the same time to ensure safe operation. The voltage DC-link is recommended to be 4 to 9 kVDC [16] or from 6 to 10 kVDC, as recommended by NASA [20]. In this model, 6 kVDC is chosen to characterise the DC-link voltage. One set of the system shown in Fig. 3.1 (one generator, one AC/DC VSC, and four motors and their VFD) has been modelled in MATLAB/Simulink Simscape block library environment to carry out the fault analysis and to perform a typical flight cycle. The ratings of the generator, motors and converters are taken based on the data of the N-3X aircraft proposed by NASA. The take-off power is 2.80 MW and the nominal rating at cruise is 1.5625 MW per motor [16].

Table 3.1: The design parameters of the TeA [16]

Parameter	Quantity	Value
Generator	4	11.20 MW, 6 kV
Motor	16	2.80 MW (≈ 2500 hp)
Converters:		
AC/DC	4	11.20 MW
DC/AC	16	2.80 MW

The modelled part of the TeA power system is shown in Fig. 3.1 and the system's components are described in Table 3.2.

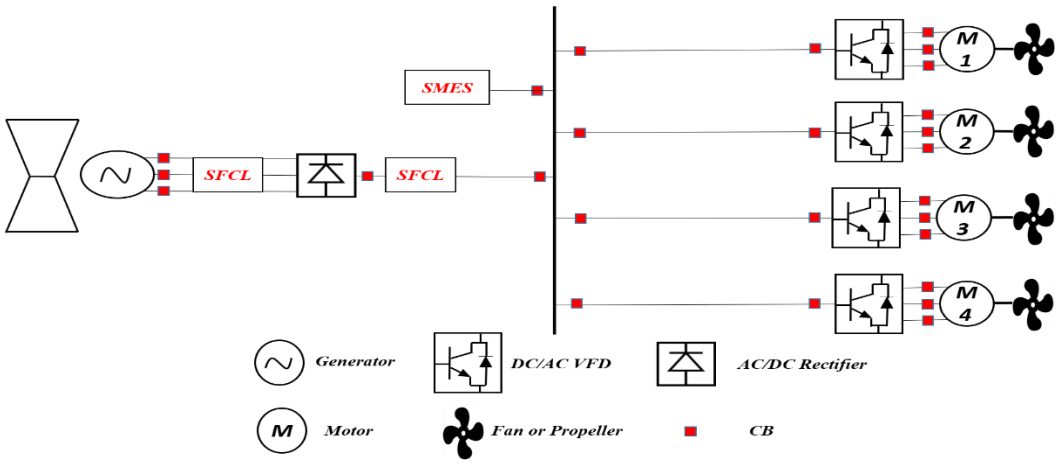


Figure 3.1: One set of the TeA with one generator, AC/DC rectifier, DC/AC inverter and four motors.

Table 3.2: The design parameters of modelled part of the TeA.

Parameter	Quantity	Value
Generator	1	11.20 MW, 6 kV
Motor	4	2.80 MW ~ rating
		2.80 MW ~ take-off
		1.5625 MW ~ cruise
Converters		
AC/DC	1	11.20MW
DC/AC	4	2.80 MW

3.2.1 Generation unit

One of the main challenges of the airborne electric microgrid of TeA is the generation unit for the propulsion system. Currently, aircraft use gas turbines (combustion engines) to produce thrust and electric generators are driven by the turbine for the secondary power systems (e.g., the avionics systems, lighting and in-flight entertainment) [123].

However, the thrust of future TeA comes from electric motors controlled by the power electronics system, and the generation unit is the source of the power for both the propulsion system as well as the secondary power systems. For the TeA power system, electric generators driven by turboshafts are the generation unit, as shown in Fig. 2.7. There are several considerations for the generator types to be used in TeA power systems, including the weight and low operation and maintenance costs. A fully superconducting machine is one of the best candidates for future electric aircraft because the superconducting machines have a higher power density (kW/kg) and torque density (N.m/kg) than conventional machines [124]. Meanwhile, aircraft use several types of generators for the secondary power systems, including AC three-phase synchronous generators, which are currently being used in Boeing 787 [125]. Permanent magnet generators are considered as an alternative due to their high power density [126]. The historical electrical demand of the aircraft is shown in Fig. 3.2. The electrical power generation in a Boeing 787 reaches over 1 MW with six generators: two on each engine and two on the auxiliary power unit. In this model, a non-salient, synchronous machine is chosen to model the characteristics of the generator. The input parameters of the

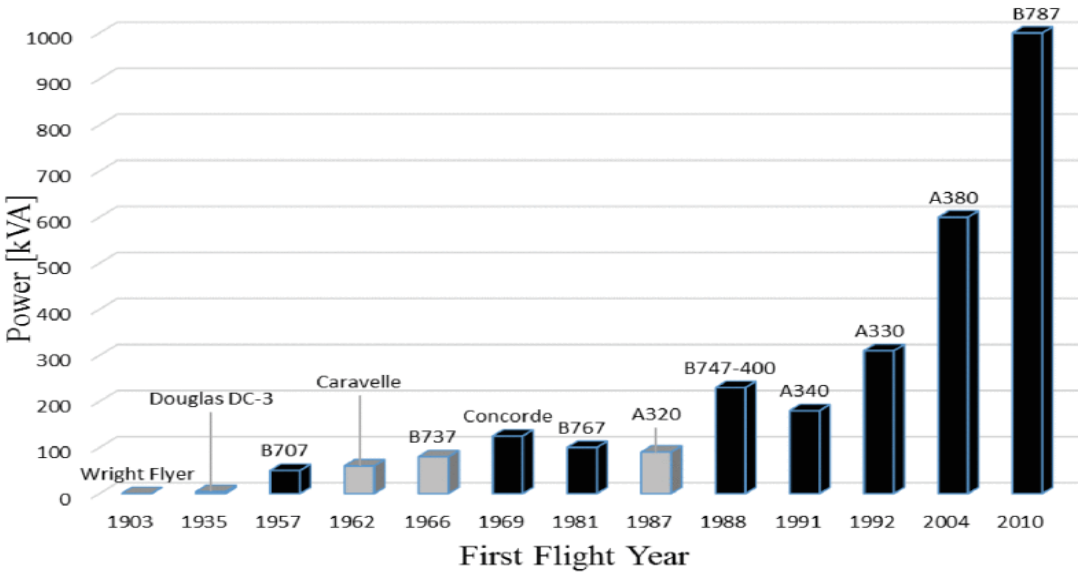


Figure 3.2 The historical power generation in aircraft [126].

generator are shown in Table 3.3. The generator is assumed to be run by a turbine at a constant speed. When the load increases, the input mechanical power increases while the speed of the generator is maintained at a constant speed. The field voltage is set as a variable to achieve a uniform rated voltage at the generator terminals.

Table 3.3: The parameters of the generator

Parameter	Symbol	Value
Rated power	P_{MAX}	11.20 MW
Rated frequency	f_{rated}	400 Hz
Rated voltage	V_{rated}	6 kV
Number of pole pairs	N	4
Inertia coefficient	H	3 s.W/VA
Stator resistance	Rs	26.86 mΩ

3.2.2 AC/DC Voltage source converter (VSC)

After the generation unit has generated the power, a rectifier is needed to convert the AC into a DC for the airborne DC microgrid, as shown in Fig. 3.1. There are mainly two types of converters: voltage source converters (VSC) and current source converters (CSC). Reversing the voltage polarity is required in the CSC, requiring an expensive and heavy cable to support the fast DC voltage reversal [23]. Because the weight is crucial in the TeA's design, the VSC topology is chosen for the rectifier in this model. Several types of VSCs mainly depend on the requirements of the system. The modular multilevel converter (MMC) has been widely investigated and is applied for HVDC applications [127]. However, because the voltage level of the TeA power system is considered as the MVDC level and the MMC technologies rely on the use of large capacitors [20], which is not desirable in a TeA, the MMC is not considered in this study. The three-level neutral-point-clamped (NPC) is considered as the second

generation of the VSCs. It has several advantages over the two-level VSC, including the reduction of the switching frequency per device, consequently reducing the switching losses, lowering the voltage potential per device, and therefore, using smaller device ratings. However, there are several challenges for three-level NPC converters, including the voltage balancing between the positive and negative poles, which is required in some cases, where an extra leg is used as a voltage balancer. Those challenges have pushed manufacturers to abandon the three-level NPC converters and focus on improving the two-level VSCs [127], [22]. The two-level VSC is chosen for this study for several reasons, including stable operation over the entire operating range with simple construction and control. It has the lowest number of switches and is therefore small in size and volume compared to the other topologies. The two-level VSC topology is shown in Fig. 3.3 (a), and the three-level NPC VSC is shown in Fig. 3.3 (b).

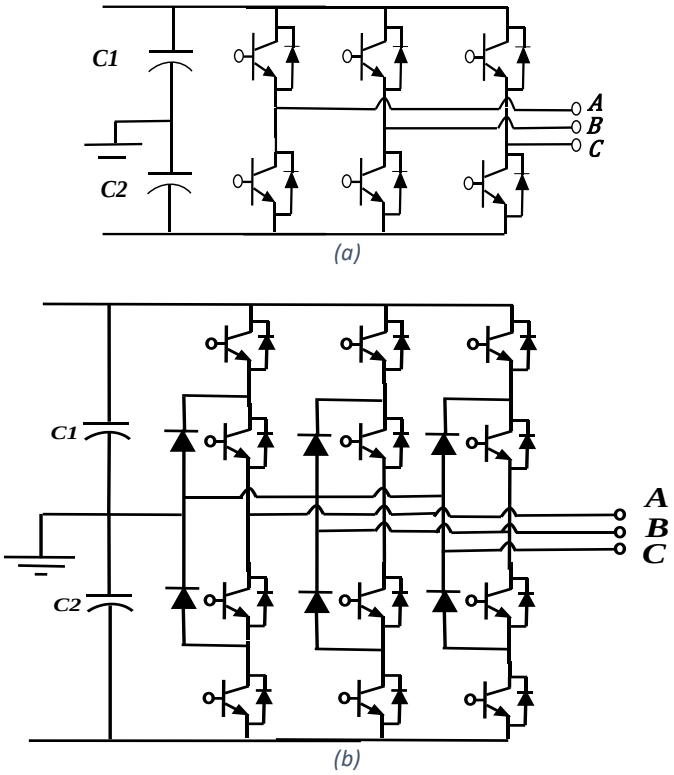


Figure 3.3: Voltage source converter topologies; (a) two-level and (b) three-level neutral point clamped.

The main purpose of the rectifier's control is to maintain the DC-link voltage at the desired level (6 kVDC). The control of the rectifier is based on double closed-loop pulse-width-modulation (PWM) based on the *d-q* axis frame, which is appropriate for medium-high voltage, large power applications [128]. The control strategy is shown in Fig. 3.4. After the conversion of the voltage from the *V_abc* to the *d-q* axis frame using park transform, the output DC voltage is compared to the voltage reference (6 kVDC) and the difference passes through a PI controller to generate the reference value of the current active component I_{d_ref}. The current reactive component I_{q_ref} reference is set to zero to achieve a unity power factor. The three-phase input current *I_abc* is converted to the *d-q* axis frame and compared with I_{d_ref} and I_{q_ref}. The error comparison is passed through a PIDs controller and then compared to both the *d-q* axis components of the input voltage and the modulated I_d and I_q values to get the output V_d and V_q values. By using inverse park transform *(d-q to abc)* and the PWM, the 6 pulses are generated to control the rectifier switching behaviour. A phase-locked loop (PLL) is used with the

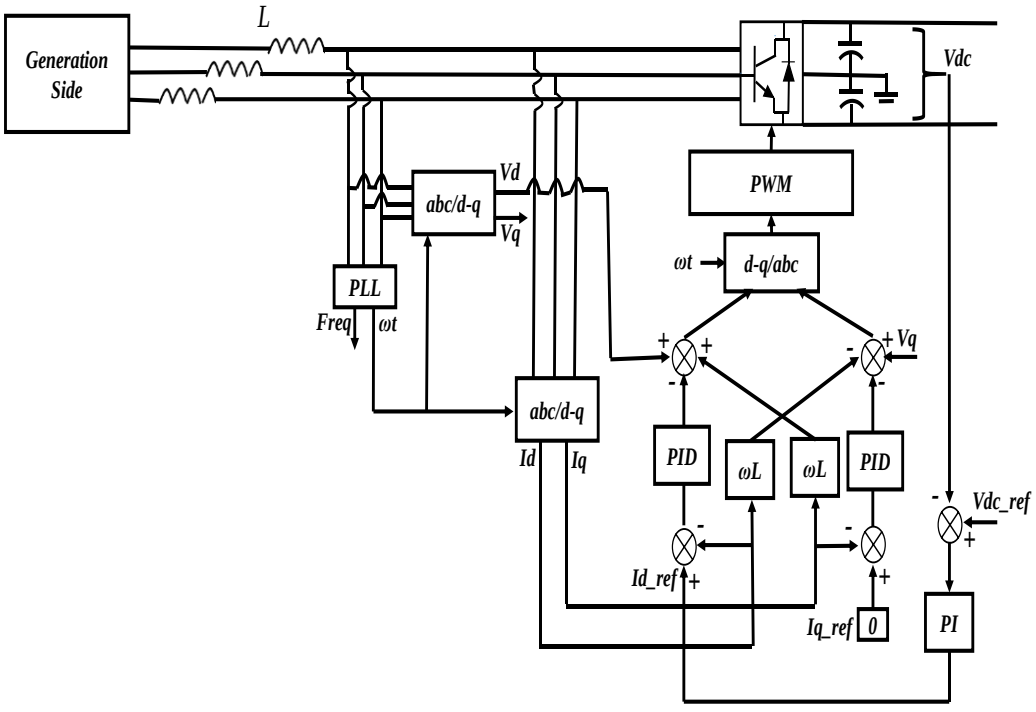


Figure 3.4: Two-level bipolar PWM rectifier control system.

park transform and the inverse park transform to keep the output signal synchronizing in phase with the reference input signal. The IGBTs on-state resistance is estimated to be 1.5 mΩ per device in the rectifier.

3.2.3 Electric propulsion system and DC/AC variable frequency drive

In this system, surface permanent magnet synchronous motors (SPMSM) are used as the electric propulsion due to their high power density and high efficiency [129]. These motors have magnets embedded into the surface of their rotors, and these magnets shape the rotating magnetic fields of the motor, and their strong magnetism results in good motor torque linearity and better control [130]–[132]. The power rating, the number of pair poles, and the nominal speed of each propulsion motor are 2.80 MW, 4, and 4000 rpm, respectively. A two-level inverter is used to control the propulsion system's speed.

The principle of controlling the motors is based on the field-oriented control (FOC) strategy, as shown in Fig. 3.5. The FOC is a VFD control method in which the stator currents of the three-phase SPMSM are converted into orthogonal components that can be visualised with a vector. The two components are defined as the magnetic flux of the motor and the torque [133]. The FOC strategy is an effective control method for synchronous motors in a wide range of speeds, including field weakening [134]. The synchronous motor under the FOC strategy is very similar to a separated excited DC motor, whereby the q-axis deals with the required torque and, consequently, the speed references, whereas the d-axis controls the magnetic flux in the stator windings. To implement the FOC strategy, the control unit translates the stator variables (currents) into a *d-q* frame coordination based on the rotor position to compare the values with the reference values ($\omega_{\_ref}$, I_{q_ref} and I_{d_ref}) and updates the PID controllers. The inverter

gate signals are updated after the back transformation of the new voltage references into the stator frame coordination and compared with the modulating signals. In order to achieve the maximum torque per ampere (MTPA) strategy, I_{d_ref} is set to zero for the whole time [135] and the gains of all PID blocks are fine-tuned by control theory analysis together with trial and error adjustments. The IGBTs on-state resistance is estimated to be 1.5 mΩ per IGBT in the inverter.

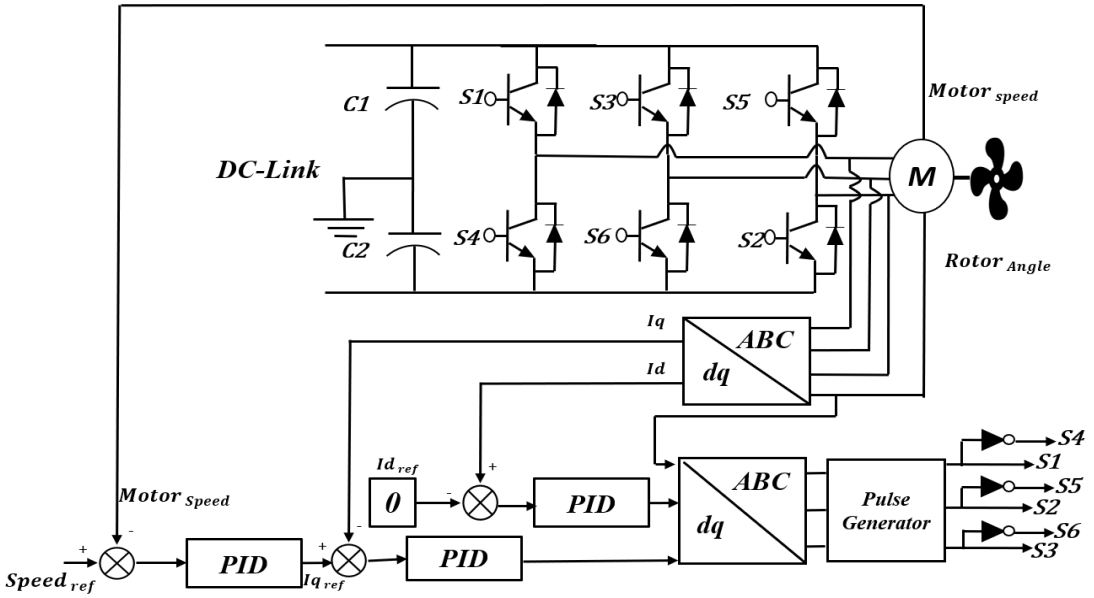


Figure 3.5: Field Oriented Control (FOC) for an electric propulsion motor.

3.2.4 Transmission lines and connectors

Because one of the main goals of modelling a TeA power system is to carry out a fault analysis, the transmission lines and connector impedances are critical components in this study. The distance from the VSC to the DC-bus is estimated to be 40 meters, whereby the distance from the DC-bus to each motor is 5 meters, based on [16]. The DC-bus voltage is 6 kVDC and each motor draws the maximum power during take-off, which is 2.80 MW. Therefore, the estimated current of the main transmission line is 1.866 kA. A 10% safety margin is added to the estimated current of the main feeder to

make the total current 2.05 kA, whereby the estimated current off each motor branch is 500 A. Two parameters should be considered to size a cable, namely the current density of the cable and the voltage drop. A copper cable with PVC insulation has a current density of 2.82 A/mm^2 [136]. In this study, a 2 A/mm^2 current density is considered for the cable. The permissible voltage drop in the MVDC power system is up to 10% [137]. As the length of the transmission line is only 40 m, the voltage drop is not at risk of exceeding the voltage drop limits. However, the current density of the cable is an issue. Based on the 2 A/mm^2 current density, the cross-section of the cable should be 1000 mm^2. The voltage drop at 1000 mm^2 is only 1.368 V, which equals 0.228%. Cable resistance and inductance are calculated using Eq. 3.1 and Eq. 3.2, respectively:

$$R_{cu} = \rho_{cu} \frac{L}{A} \tag{3.1}$$

$$L_{wires} = \frac{\mu_0 \mu_r}{\pi} cosh^{-1}\left(\frac{s}{d}\right).L \tag{3.2}$$

Where ρ_{cu} is the resistivity of copper at 20^0 C (1.7241x10^{-8}ohm-meter), L is the cable length in meters and A is the cross-sectional area of the cable in squared meters. μ_0 is the permeability of free space, μ_r is the relative permeability, s is the distance between the wires, d is the wire diameter, and L is the wire length. Based on the above equations, the transmission line impedance is 17.241 mΩ/km and 0.403 mH/km. The feeder line cable cross-sectional area is calculated to be 300 mm^2 with 56 mΩ/km and 0.491 mH/km.

3.3 A typical flight cycle

A typical flight cycle is an attractive topic for aircraft electrification due to the tremendous opportunities for optimization and efficiency improvement of the propulsion unit [138]. However, the main goal of this section is to demonstrate the behaviour of the modelled system by showing the flight cycle of the modelled system during different flight stages, i.e. taxi, take-off, top of climb, cruise, top of descent and landing. The behaviour of the voltage, current, and motor speed during a typical flight cycle are shown in this section. The power demand of a typical flight cycle according to Rolls-Royce is shown in Fig. 3.5. The typical flight cycle of the distributed electrical aerospace propulsion (DEAP) project is shown in Fig 3.6.

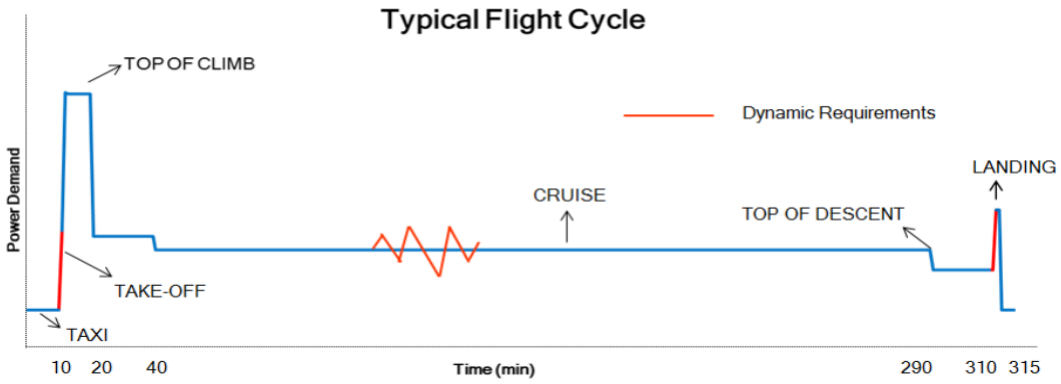


Figure 3.5: Typical flight cycle according to Rolls-Royce [139].

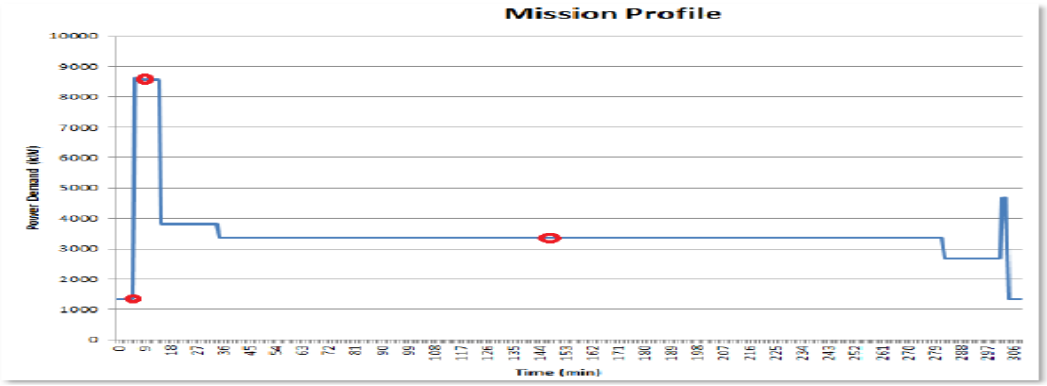


Figure 3.6: Flight cycle for the DEAP aircraft [138].

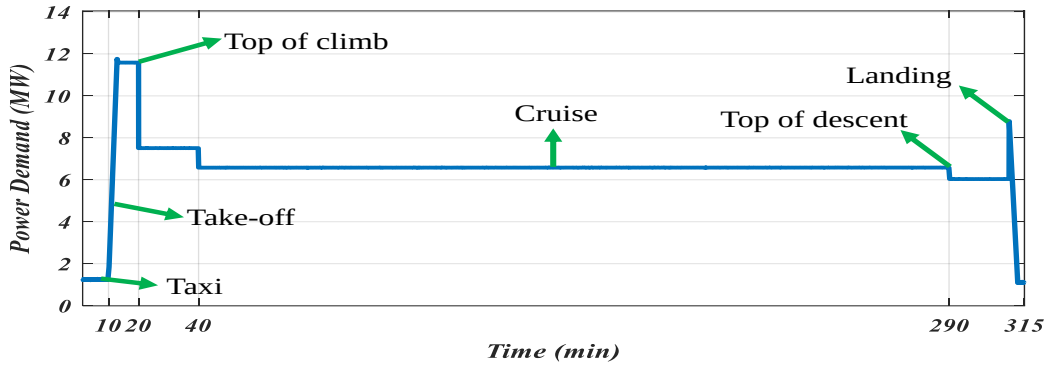


Figure 3.7: Typical flight cycle based on modelled TeA.

Fig. 3.7 shows the typical flight cycle of one set of the system, as shown in Fig. 3.1. The following equations can calculate the power demand of the system:

$$P = V \times I \tag{3.3}$$

$$P = T_e \omega_{rm} + P_{loss} \tag{3.4}$$

Where the voltage and current are measured in the transmission line, T_e is the electrical torque of the motor in N.m, and ω_{rm} is the rotor speed in rad/sec. The voltage and the current of the transmission line are shown in Fig. 3.8 and 3.9, respectively.

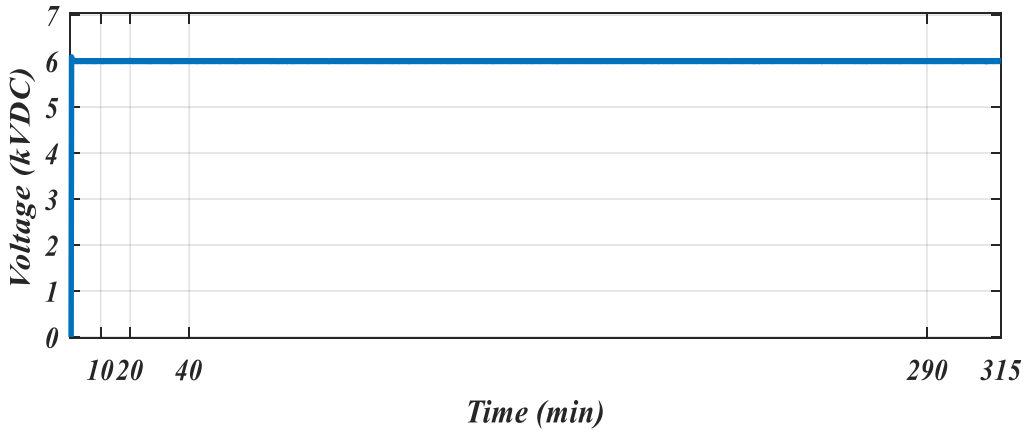


Figure 3.8: DC-link Voltage.

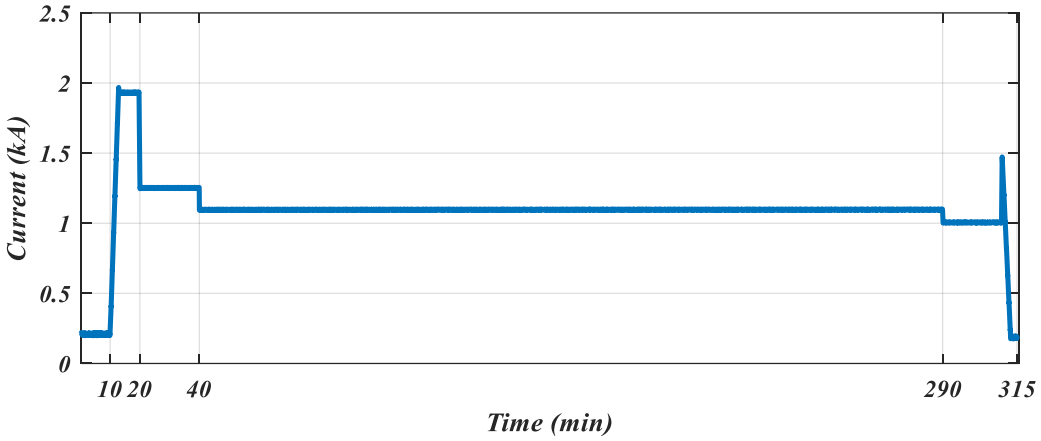


Figure 3.9: Current at the transmission line of the TeA set.

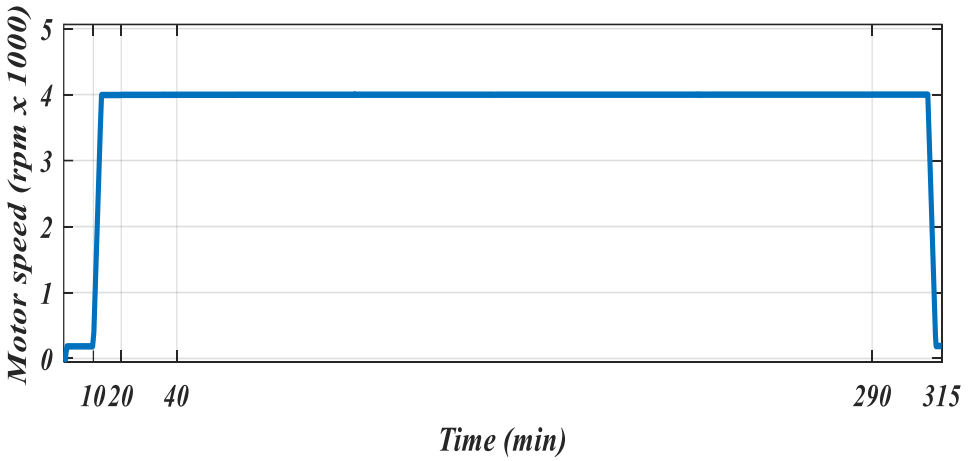


Figure 3.10: Propulsion speed for one motor.

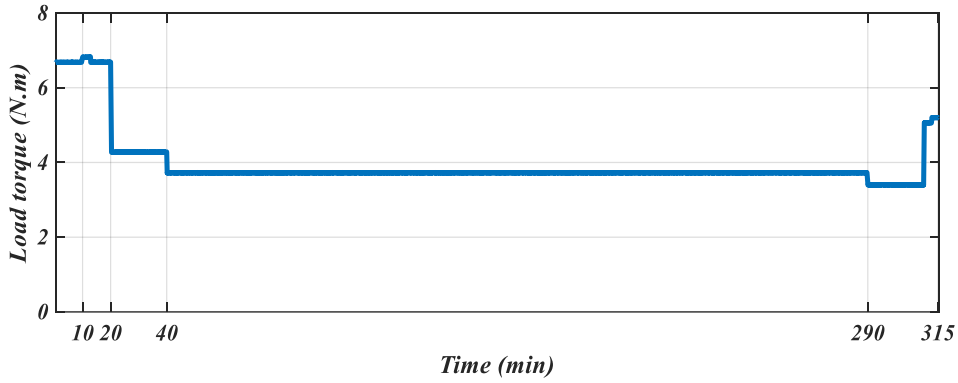


Figure 3.11: Propulsion load torque for typical flight cycle

The electrical torque and the rotor speed of the propulsion unit motor are shown in Fig. 3.10 and 3.11, respectively.

3.4 Chapter summary

Chapter 3 described the platform of this study, namely one set of the TeA power system architecture, including one generator, one AC/DC VSC , transmission lines/connectors, and four motors and their VFDs. A typical flight cycle based on the modelled system was presented to demonstrate the performance of the system's components. The power demand, voltage, current and motor speeds were observed.

Based on this model, the fault analysis is conducted in Chapter 4 for different locations in the TeA power system and with different grounding materials and different voltage levels.

Chapter Four

4. DC Fault Analysis for Turboelectric Aircraft

4.1 Introduction

In this chapter, the DC fault characteristics of the TeA power system are described, and fault analysis is carried out at two different voltage levels; 6 kVDC and 9 kVDC, and as such different DC-link capacitors and line impedances are used. In addition, two types of grounding with different impedances are used; metallic airframe (aluminium alloy) which is considered low grounding impedance and CFRP, which is considered high grounding impedance. The two voltage levels (6 and 9 kVDC) are chosen based on DC voltage level recommendations from NASA's TeA reports [16], [20].

Fault analysis is a critical aspect in power system design, more so with critical and sensitive loads directly tied to human safety, as they are in aircraft. Fault analysis helps with determining many parameters concerning fault currents, including magnitude, rise time, effect on system stability, and more, allowing for more effective designs of protection systems to ensure safe and stable operation even during unexpected faults. Because the TeA has an airborne DC-microgrid, understanding how faults behave and how the network responds in such a case results in better designs, thus leading to a highly resilient and well-protected network that can withstand unexpected faults.

Although there are several advantages for DC microgrids over AC ones as mentioned earlier, fault protection in DC distribution systems is a significant challenge due to the higher fault currents and the absence of zero-crossing points [21], [22]. There are several factors that determine fault characteristics, including voltage levels, DC-link capacitance, line impedance, and grounding impedance [23], [24].

Several studies have discussed fault analysis for DC microgrids. Cable faults are analysed for traditional DC network VSC-based with different distances [140]. Pole-to-pole faults are analysed for unmanned aerial vehicle (UAV) low voltage DC (LVDC) system to determine the protection requirements and to enhance the capability and survivability of the microgrid and the protection systems [141]. DC microgrid fault analysis and protection requirements are discussed in [22] and [142].

4.2 DC fault characteristics

In this section, DC pole-to-pole and pole-to-ground faults are analyzed. The more catastrophic but rarer of the two is the pole-to-pole fault due to its higher voltage potential. Meanwhile, pole-to-ground faults are comparatively less hazardous but are much more likely to happen. Pole-to-pole faults occur due to direct contact or insulation failure between the positive and negative conductors of a DC line, while the pole-to-ground fault occurs when one of the conductors makes direct contact to the ground, which is the airframe in the case of aircraft (CFRP/metallic) [58], [59].

Due to the naturally compact DC microgrid of the TeA, the charged DC-link capacitors act as high fault current sources. In additions, the short line impedances of the network create conditions for potentially severe faults which is not the case in other DC applications where longer and higher impedance lines are utilized.

4.2.1 Pole-to-pole fault

When the DC pole-to-pole fault occurs, the fault current behaves in a nonlinear way. The nonlinear behaviours can be divided into three stages. The three stages of the fault are described individually in the following sub-sections, and are all shown in Fig. 4.1.

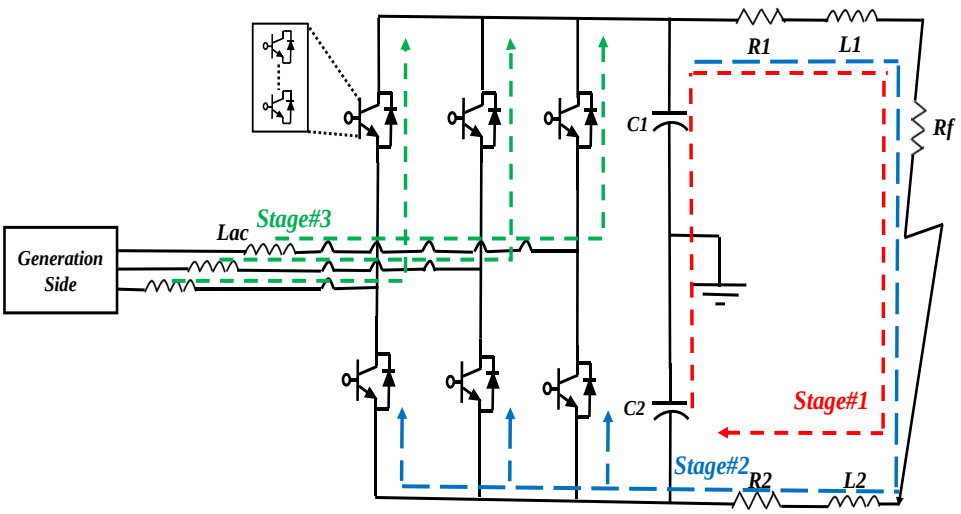


Figure 4.1: Equivalent scheme of VSC under pole-to-pole fault condition.

4.2.1.1 Capacitor discharge stage (natural response)

When the pole-to-pole fault occurs in the DC side, the DC-link charged capacitors start discharging through the cables (i.e. the red path in Fig. 4.1). The peak value of the fault occurs at this stage and can reach hundreds of times of the rated DC current, depending on the voltage level, capacitors, cable impedances and grounding impedance. The equivalent circuit of this stage is represented in Fig. 4.2, and by applying Kirchhoff's voltage law, the equivalent equation of the circuit is as shown in Eqs. 4.1, 4.2:

$$V_R(t) + V_L(t) + V_C(t) = 0 \tag{4.1}$$

$$i(t)R + L\frac{di(t)}{dt} + \frac{1}{C}\int_0^{\tau} i(t) - V_C(0) = 0 \tag{4.2}$$

Where R is the sum of the resistances of both lines connecting the VSC to the location of the occurring fault, while L is the sum of the inductances of the same lines. C in these equations is the equivalent capacitance. $V_C(0)$ is the initial voltage across the capacitor. By converting Eq. 4.2 to Laplace transform $I(s)$ can be found by Eq. 4.4.:

$$I(s)R + L[sI(s) - I_L(0)] + \frac{I(s)}{sC} - \frac{V_C(0)}{s} = 0 \tag{4.3}$$

$$I(s) = \frac{\frac{V_C(0)}{L} + I_L(0)s}{s^2 + \left(\frac{R}{L}\right)s + \left(\frac{1}{LC}\right)} \tag{4.4}$$

where $I_L(0)$ is the initial current through the inductors.

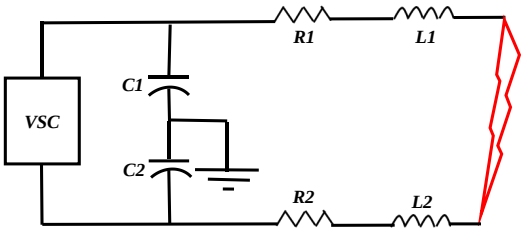


Figure 4.2: Equivalent circuit of pole-to-pole fault condition first stage.

Taking the inverse Laplace transform of Eq. 4.4, the general current representation in the time domain is shown in Eq. 4.5:

$$i(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t} \tag{4.5}$$

where $A_{1,2}$ are coefficients which depend on initial conditions and $S_{1,2}$ are the roots of the characteristic equation which are calculated in Eq. 4.6:

$$s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2} \tag{4.6}$$

Where α is the damping factor and ω_0 is the resonant radian frequency and they can be calculated by Eq. 4.7 and Eq. 4.8, respectively:

$$\alpha = \frac{R}{2L} \tag{4.7}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{4.8}$$

The current response behaviour can be determined by Eq. 4.9 as the follows:

$$\begin{cases} \alpha^2 > \omega_0^2, & over-damped \\ \alpha^2 = \omega_0^2, & critically-damped \\ \alpha^2 < \omega_0^2, & under-\ damped \end{cases} \tag{4.9}$$

A_1 and A_2 of Eq. 4.5 can be calculated by Eq. 4.10 and Eq. 4.11:

$$A_1 = \frac{\frac{V_C(0)}{L} + s_1 i_L(0)}{(s_1 - s_2)} \tag{4.10}$$

$$A_2 = \frac{\frac{V_C(0)}{L} + s_2 i_L(0)}{(s_2 - s_1)} \tag{4.11}$$

By substituting Eq. 4.10 and Eq. 4.11 in Eq. 4.5, the fault current $i(t)$ can be calculated by Eq. 12:

$$i(t) = \frac{\frac{V_C(0)}{L} + s_1 i_L(0)}{(s_1 - s_2)} e^{s_1 t} + \frac{\frac{V_C(0)}{L} + s_2 i_L(0)}{(s_2 - s_1)} e^{s_2 t} \tag{4.12}$$

Because the TeA is a compact network with a large DC-link capacitance and a relatively low line impedance, the dominant part of Eq. 4.12 is the initial voltage across the capacitance $V_C(0)$, thus for manual calculation, $i(t)$ can be simplified as in Eq. 4.13:

$$i(t) = \frac{V_C(0)}{L(s_1 - s_2)} [e^{s_1 t} - e^{s_2 t}] \tag{4.13}$$

And the peak time of the fault can be calculated by Eq. 4.14:

$$t_{peak} = \frac{\ln\left(\frac{s_2}{s_1}\right)}{(s_1 - s_2)} \tag{4.14}$$

Eq.14 is used in the result section to compare the theoretical values with the simulation results, where Eq. 4.13 and Eq. 4.14 can be used for manual calculations.

4.2.1.2 Diode freewheeling stage ($V_C(0) = 0$; Natural Response)

The diode freewheeling stage occurs when the DC-link capacitors discharge completely and the voltage of the DC-link capacitor $V_C(0)$ reaches zero. This occurs when the power source is lost at any point during the fault response process and is usually during the underdamped fault response. In this case, the cable current commutates to the VSC freewheeling diodes (i.e. the blue paths in Fig. 4.1). Thus, the currents in the cable and in each leg can be calculated by Eq. 4.15 and Eq. 4.16, respectively:

$$I_{cable} = I'_0 e^{-(\frac{R}{L})t} \tag{4.15}$$

$$I_{D1} = \frac{I_{cable}}{3} \tag{4.16}$$

The initial cable current I'_0 is the remaining inductive energy in the system when capacitor voltage is zero. I'_0 can be ten times the nominal current value if the dissipative loss in the system is very low. Thus, the freewheeling diodes are at high risk of damage if this stage lasts for a long time. Therefore, it is highly desirable to detect and isolate the fault in the first stage (capacitor discharge stage).

4.2.1.3 Generation-side current feeding stage

In this stage, the VSC acts like an uncontrollable full-bridge rectifier and contributes to the fault current through the freewheeling diodes as shown by the third stage path in Fig. 4.1 (the green path). The fault current in this stage can be represented by Eq. 4.17:

$$i_{VSC} = i_{D1} + i_{D2} + i_{D3} \tag{4.17}$$

Where i_{D1}, i_{D2} and i_{D3} are the positive values of phase a, b and c currents passing through the freewheeling diodes.

4.2.2 Pole-to-ground fault

The pole-to-ground fault is more likely to happen in DC systems. Here, either the positive pole or the negative pole will have direct contact to the ground, i.e. the airframe in this study. When the fault occurs, the DC-link capacitor of the faulted pole, the line impedance of the faulted pole, and the impedance of the grounding path (i.e. the metallic or CFRP airframe) will form a loop as shown in Fig. 4.3. The fault behaviour can be divided into three stages.

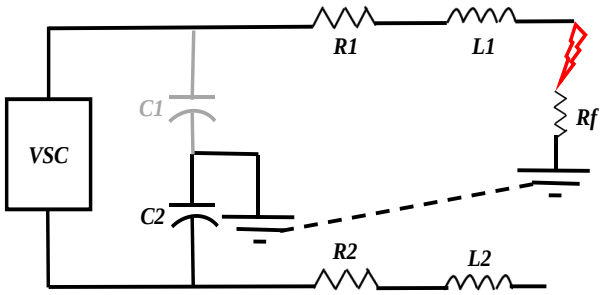


Figure 4.3 :Equivalent circuit of the third stage of the pole-to-ground fault.

4.2.2.1 Capacitor discharge stage ($V_C(0) = 0$; Natural Response)

When the pole-to-ground fault occurs, the capacitor starts discharging through the faulted pole's impedance, the ground and up to the mid-point of the DC-link capacitors. The voltage of the faulted pole rapidly approaches zero.

The equivalent circuit of the pole-to-ground fault is shown in Fig. 4.3 and by using the same approach in pole-to-pole fault, $i(t)$ can be calculated by the following Eq 4.18:

$$i(t) = \frac{\frac{V_C(0)}{L} + s_1 i_L(0)}{(s_1 - s_2)} e^{s_1 t} + \frac{\frac{V_C(0)}{L} + s_2 i_L(0)}{(s_2 - s_1)} e^{s_2 t} \tag{4.18}$$

$$s_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2} \tag{4.19}$$

$$\alpha = \frac{R}{2L} \tag{4.20}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{4.21}$$

Where $R=R_1+R_f$, $L=L_1$ and $C=C_1$.. In addition, the initial value of $V_C(0)$ here is half of the initial value of the pole-to-pole fault. The main damage that the pole-to-ground fault can cause in this stage is that the healthy pole voltage would rise to twice its rated voltage which can damage the insulation system of the lines. The peak value of the fault also occurs at this stage. The fault response behaviours can be determined by α and ω_0 relationship as shown in Eq. 4.22.

$$\begin{cases} \alpha^2 > \omega_0^2, & over-damped \\ \alpha^2 = \omega_0^2, & critically-damped \\ \alpha^2 < \omega_0^2, & under-\ damped \end{cases} \tag{4.22}$$

The case here depends primarily on the ground resistance R_f, which is controlled by the airframe (Metallic/CFRP). The current can be over-damped with high grounding impedance and can be under-damped with low grounding impedance. The end of this stage will happen when the voltage across the faulted capacitor drops to zero and the voltage of the healthy pole rises to double its nominal voltage.

4.2.2.2 Generation-side current feeding stage

This stage starts when the DC voltage drops to below any grid phase voltage, as the system will experience the grid-side current feeding stage. The VSC acts like an uncontrollable full-bridge rectifier and contributes to the fault current through the freewheeling diodes. The fault current in this stage can be represented by Eq. 4.23:

$$i_{VSC} = i_{D1} + i_{D2} + i_{D3} \tag{4.23}$$

Where i_{D1}, i_{D2} and i_{D3} are the positive values of phase a, b and c currents passing through the freewheeling diodes. This stage will end when the DC voltage becomes higher than the AC phase voltage (i.e. when the DC voltage recovers).

4.2.2.3 Voltage recovery stage

During this stage, the faulted pole's capacitor is continuously discharging through the fault, the charging current provided by the VSC is charging the non-faulted pole capacitor through the ground as shown in Fig. 4.3. When the voltage of the healthy pole is doubled, the voltage of the faulted pole becomes zero, as a result, no current will feed the fault because the voltage between the faulted pole and the ground is zero. If the voltage insulation is not designed properly, the voltage insulation may fail in the healthy pole due to the doubled voltage.

4.2.2.4 Grounding in turboelectric aircraft DC system

As the power system architecture used in this study is a DC power system based on the proposed architecture in NASA report, the grounding system will be based on a positive pole, a negative pole as a return path, and the ESN in the airframe as a ground, as shown in Fig. 4.4. The pole-to-pole fault is not affected by the different airframe or grounding technique because the return path of the fault is the negative pole. However, such changes greatly affect pole-to-ground faults as will be demonstrated in this chapter, with the aluminum airframe constituting a low grounding impedance (<0.1 Ω), while the CFRP airframe results in a high grounding impedance (from few to tens of ohms, depending on the position of grounding points, orientation with respect to the cable, etc.) [143].

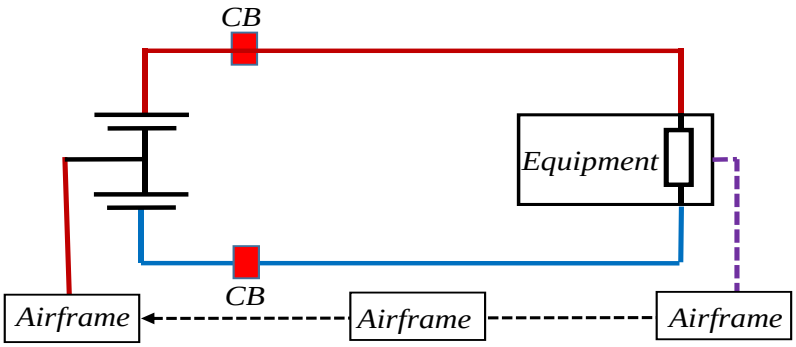


Figure 4.4: Grounding in aircraft DC system.

4.3 Case 1 – 6 kV DC-link

In order to carry out the fault analysis, the airborne DC-microgrid as shown in Fig. 4.5 has been modelled in MATLAB®/ Simulink Simscape library. In this power system architecture, the protection system is supressed to showcase fault behaviour and a system response. The voltage level of the DC-link is 6 kVDC as recommended by NASA for TeA [16]. The DC-link capacitor is calculated by Eq. 4.23 [144]:

$$C_{dc} = \frac{2SE_{dc}}{V_{dc}^2} \tag{4.23}$$

Where C_{dc} is the DC-link capacitance, S is the converter's MVA rating, V_{dc} is the rated DC voltage (6 kVDC in this case study). E_{dc} is the energy to power ratio in practical converters. E_{dc} ranges from 10 kJ/MVA to 50 kJ/MVA which is considered as a good trade-off between harmonic penetration and control performance [144]. E_{dc} is assumed to be 30 kJ/MVA in this case study. Based on Eq. 4.23, the pole to neutral DC capacitor for the 11.20 MW, 6 kVDC system is 40.3 mF.

The line impedances are calculated based on the cable size, cable material, cable distance and the space between outgoing and incoming cables. The respective cable impedances were calculated in section 3.2.4 by Eqs. 3.1 and 3.2 to be 17.241 mΩ/km and 0.403 mH/km for the transmission line and 56 mΩ/km and 0.491 mH/km for the

feeder lines. Fig. 4.5 shows the TeA power system architecture with the locations of Fault #1 and Fault #2. The 6 kVDC TeA system components are shown in Table 4.1. The VFD capacitors are chosen to limit the system's ripples to within 5%.

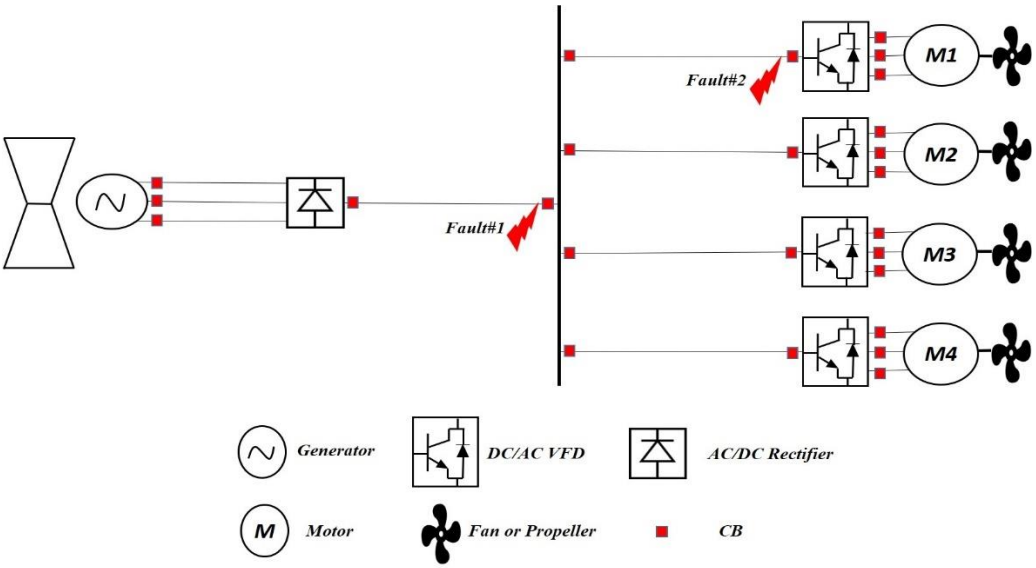


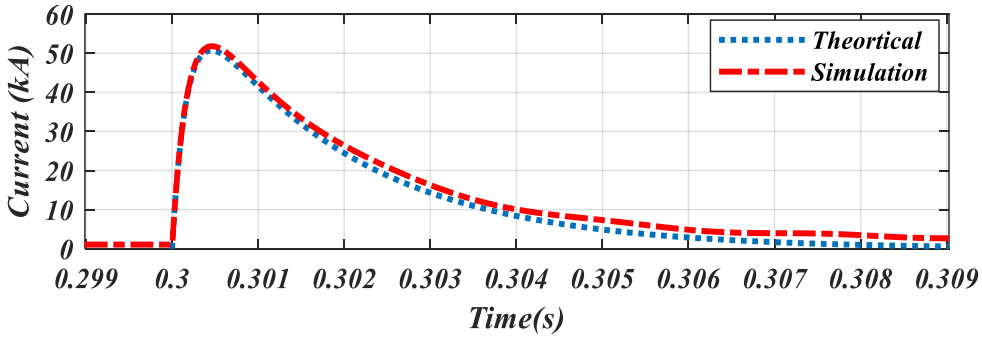
Figure 4.5: One set of the TeA including the two fault locations; Fault #1 and Fault #2.

Table 4.1: TeA architecture components for 6 kVDC system.

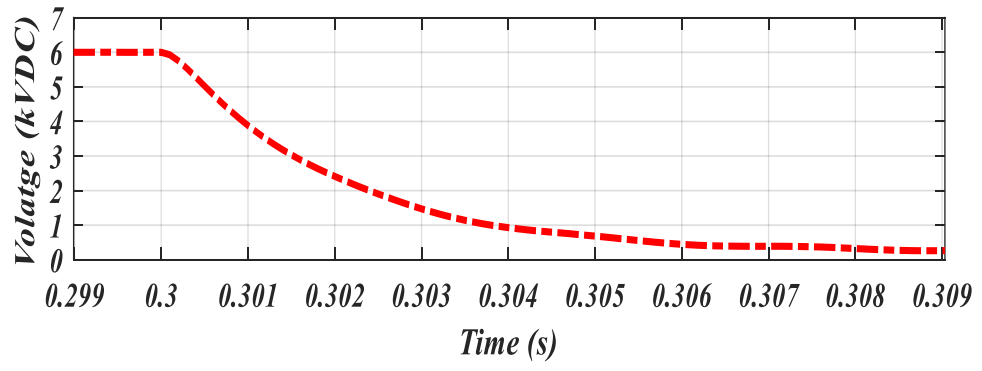
Parameter	Quantity	Value
Generator	1	11.20 MW, 6 kV
Motor	4	2.80 MW ~ rating
		1.5625 MW ~ cruise
Converters:		
AC/DC	1	11.20 MW
DC/AC	4	2.80 MW
Cables:		
Transmission	1 (40 m)	XLPE copper, 1000 mm^2
		17.241 mΩ/km,0.403 mH/km
Feeder	4 (5 m)	XLPE copper, 300 mm^2
		56 mΩ//km, 0.491 mH/km
DC-link capacitor	2	40.3 mF
VFD Capacitor	8	2 mF

4.3.1 Pole-to-pole fault

The pole-to-pole fault occurs when the positive pole is directly connected to the negative pole. The pole-to-pole fault is applied to the modelled system at the location of Fault #1 as shown in Fig. 4.5 at t=0.3 sec. Fig. 4.6 (a) compares the fault current of the simulated system to the theoretical calculation. The simulation system was built in MATLAB®/Simulink Simscape environment, whereas the theoretical values were calculated using a MATLAB® code that implemented the mathematical analysis shown in the previous section. The mathematical code is shown in Table 4.2. The fault current of the simulation system reaches 51.8 kA which is 27 times the rated current during take-off (1.92 kA). The simulation results and the theoretical values show great agreement in the same figure. The voltage of DC bus drops to almost zero within a few milliseconds as shown in Fig. 4.6 (b).



(a)



(b)

Figure 4.6: Pole-to-pole 6 kVDC Fault #1: (a) current in kA simulation and theoretical values(b) DC bus voltage.

Table 4.2: Code used to calculate the fault based on the mathematical analysis for pole-to-pole fault.

```
%%Theoretical calculation for pole-to-pole fault
%%6kVDC Fault#1
t =(0:0.00001:0.1);
t1=t+0.3;
R=0.1013;                          %% Total resistance
L=16.12e-6;                        %% Total inductance
C=20.15e-3;                        %% Total capacitance
Vc=6000;                           %% Initial voltage
Il=1080;                           %% Initial current
a=R/(2*L);                         %% Damping factor
w=1/sqrt(L*C);                     %% Resonant radian frequency
s1=-a+(sqrt(a^2-w^2));             %% s1 Root of Eq 4.6
s2=-a-(sqrt(a^2-w^2));             %% s2 Root of Eq 4.6
A1=((Vc/L)+(s1*Il))/(s1-s2);       %% Eq 4.10
A2=((Vc/L)+(s2*Il))/(s2-s1);       %% Eq 4.11
I=A1*(exp(s1*t))+A2*(exp(s2*t));   %% Eq 4.12 Current
plot (t1,I)                        %% Plot current (theoretical
                                   analysis)
hold on
plot(I_6_PP_1(:,1),I_6_PP_1(:,2))%% Plot current (simulation
                                   result)
hold off
%%End
```

The pole-to-pole fault is applied in the second location (Fault #2) as shown in Fig. 4.5 at t=0.3 sec. Fig. 4.7 (a) shows the current at the faulty feeder. Fig. 4.7 (b) shows the DC bus voltage. Fig. 4.7 (c) shows the speed of motor M4 during the fault. The peak fault current was taken on the feeder of M1 as shown in Fig. 4.7 (a). In the zoomed-in view in Fig 4.7 (a), it is clear that the fault current has two peaks which are 50.8 kA and the second is 54 kA. The first peak is dominated mainly by contribution from the VFD capacitors due to the short distance between them and the fault location (10 m), while the second peak is dominated by the VSC's capacitors. The voltage of the DC bus drops to almost zero within a few milliseconds, as shown in Fig. 4.7 (b). As a result, the speed of motor M4 dropped to zero accordingly as shown in Fig. 4.7 (c).

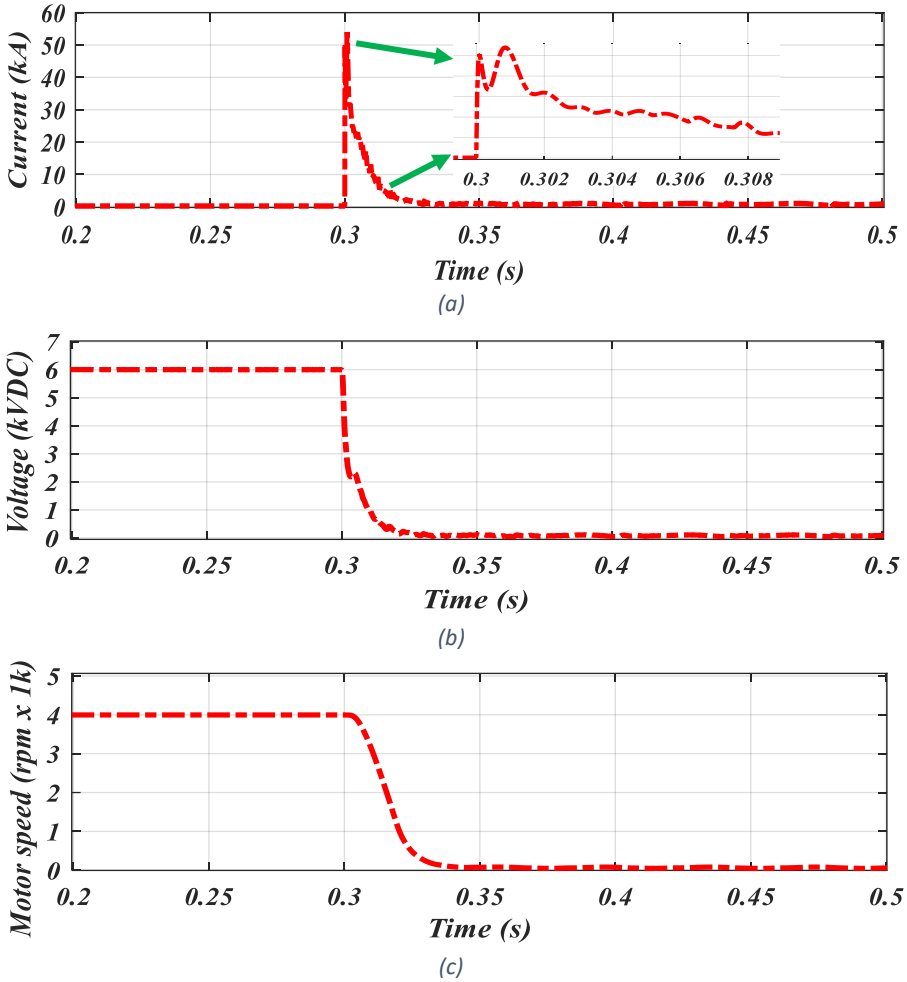


Figure 4.7: Pole-to-pole fault in 6 kVDC system at Fault #2: (a) current in kA (b) DC bus voltage (c) M4 motor speed.

4.3.2 Pole-to-ground low grounding impedance fault (Metallic)

The pole-to-ground fault occurs when one of the poles touches the ground (airframe) directly. The airframe in this case is considered to be metallic (aluminum alloys) with low grounding impedance, estimated to be 0.1 Ω. Fig. 4.8 (a) shows the simulated and theoretical fault currents, the fault current reached 28.05 kA which is 25.5 times the rated current. The simulated and theoretical results show great agreement here as well. The generation-side current feeding in this case lasts till 0.35 sec, when the voltage recovers completely as shown in Fig 4.8 (b). At that point, the faulted pole voltage becomes zero, meaning that no current flows from the faulted pole to the ground, and

the voltage on the negative pole becomes –6 kVDC. The code for the theoretical calculation is shown in Table 4.3.

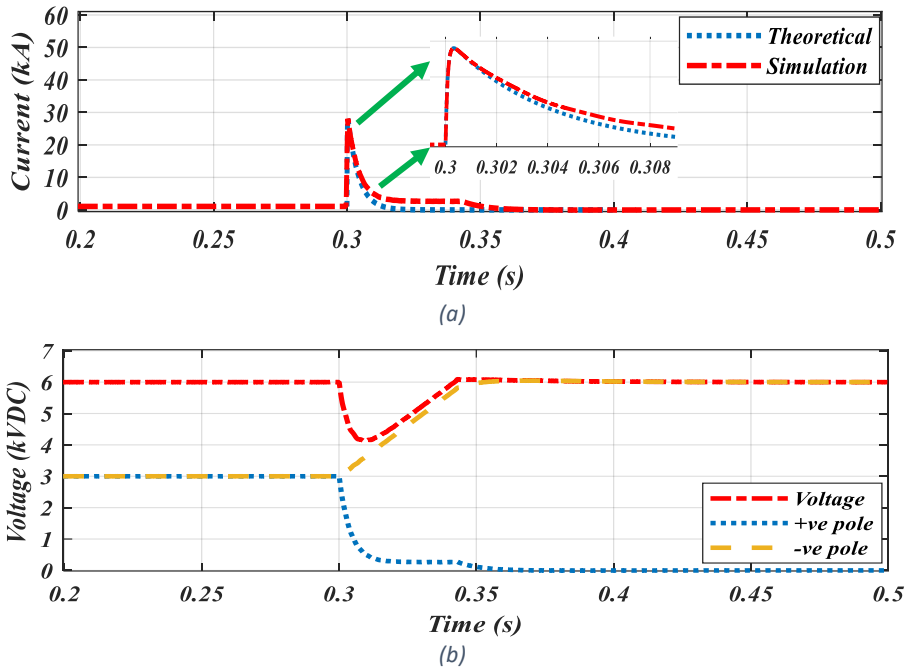
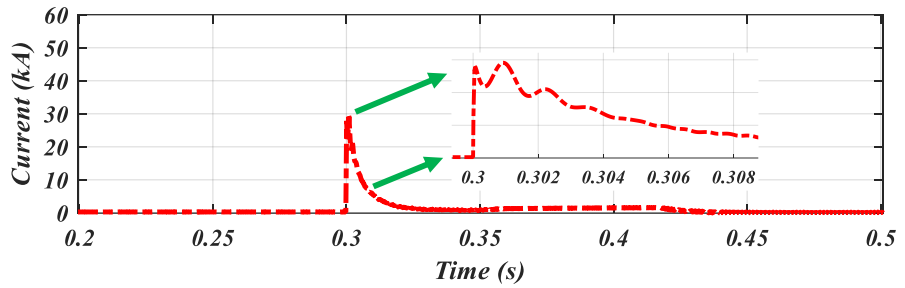


Figure 4.8: Pole-to-ground fault in the 6 kVDC low grounding impedance system Fault #1: (a) current in kA (b) DC bus voltage.

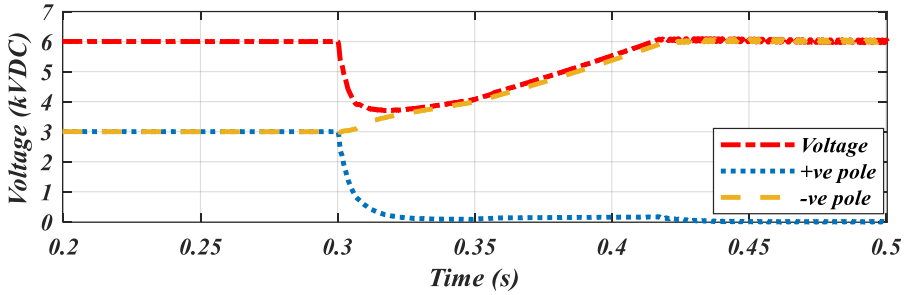
Table 4.3: Code used to calculate the fault based on the mathematical analysis for pole-to-ground fault.

```
%%Theoretical calculation for pole-to-ground fault
%%6kVDC Fault#1
t =(0:0.00001:0.1);
t1=t+0.3;
R=0.10068;                          %% Total resistance
L=8.06e-6;                          %% Total inductance
C=40.3e-3;                          %% Total capacitance
Vc=3000;                            %% Initial voltage
Il=1080;                            %% Initial current
a=R/(2*L);                          %% Damping factor
w=1/sqrt(L*C);                      %% Resonant radian frequency
s1=-a+(sqrt(a^2-w^2));              %% s1 Root of Eq 4.19
s2=-a-(sqrt(a^2-w^2));              %% s2 Root of Eq 4.19
A1=((Vc/L)+(s1*Il))/(s1-s2);        %% Eq 4.10
A2=((Vc/L)+(s2*Il))/(s2-s1);        %% Eq 4.11
I=A1*(exp(s1*t))+A2*(exp(s2*t));    %% Eq 4.18 Current
plot (t1,I)                         %% Plot current (theoretical
                                    analysis)
hold on
plot(I_6_PG_Low_1(:,1),I_6_PG_Low_1(:,2))%% Plot current
                                          (simulation result)
hold off
%%End
```

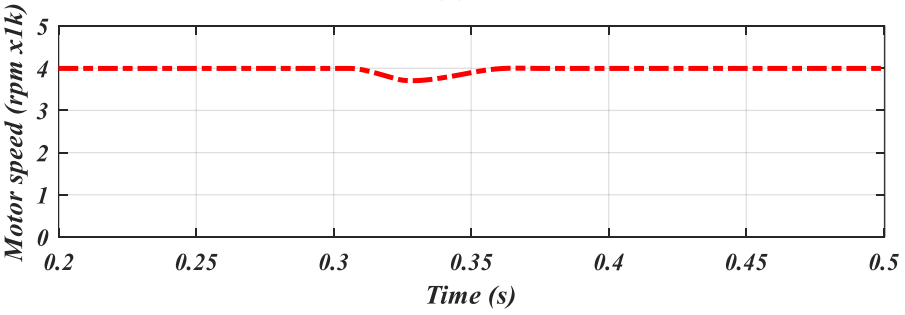
The same fault is applied on the feeder line of motor M1 as shown in Fig. 4.5. Fig. 4.9 (a) shows the current at the faulty feeder. Fig. 4.9 (b) shows the DC bus voltage. Fig. 4.9 (c) shows the speed of motor M4 during the fault. The fault current has two peaks, the first of which is 27.8 kA and the second is 29.1 kA due to the contribution of the VFD capacitors to the fault. The fault current in the first stage of the fault reached almost 29.1 kA which is 40.3 times the rated current. The recovery stage of the DC bus lasts for 120 msec as shown in Fig. 4.9 (b). As a result, the motor speed (M4 here specifically) has a short drop to 3.7k rpm for a few milliseconds before recovering, as shown Fig. 4.9 (c).



(a)



(b)



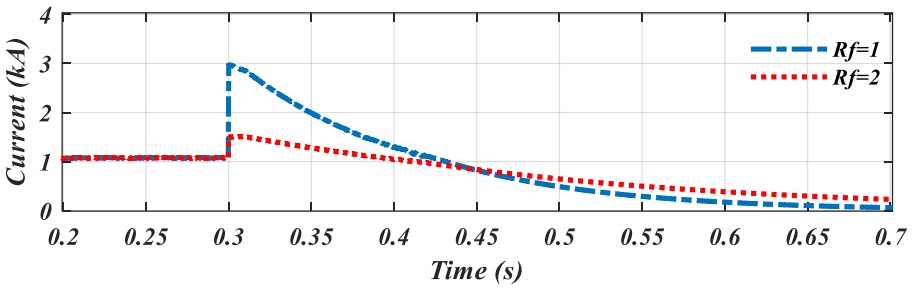
(c)

Figure 4.9: Pole-to-ground 6kVDC low grounding impedance Fault #2: (a) current in kA (b) DC bus voltage (c) M4 motor speed.

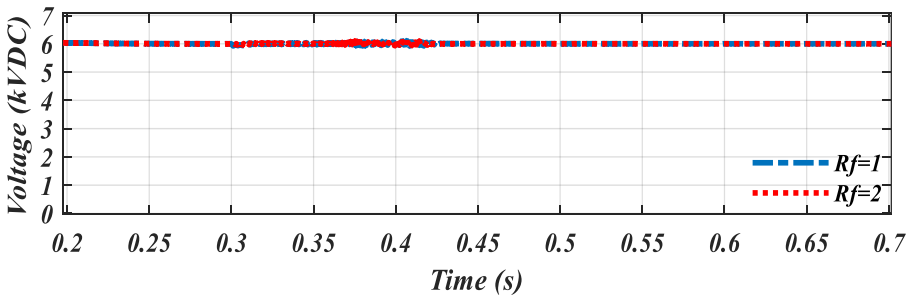
4.3.3 Pole-to-ground high grounding impedance fault (CFRP)

The same fault is applied to the system with high grounding impedance (CFRP). According to [143], the resistance of the CFRP can range from a few Ohms to ten Ohms. Two different grounding impedances are considered in this case study; R_{f1}=1Ω, and R_{f2}=2Ω. Fig. 4.10 (a) shows the fault current of the two different grounding cases, and fault current peaks are 3 kA and 1.5 kA for R_{f1}=1Ω and R_{f2}=2Ω , respectively.

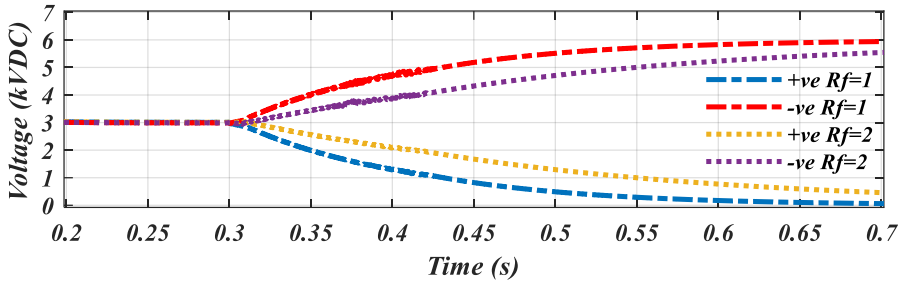
The abnormal fault current lasted only for ~100 msec and then the current decreased to reach to zero as the positive pole's voltage dropped to zero. Fig. 4.10 (b) shows the DC bus voltage in the two different cases. On the DC bus, the two voltages were stable and that is due to the change of the pole voltages as shown in Fig. 4.10 (c). The rated current of the transmission line at take-off is 1.92 kA. If the fault current is less than the rated current at take-off, the detection of the fault is not possible by traditional fault detection techniques. More discussion will be done in Chapter 6 about fault detection techniques.



(a)



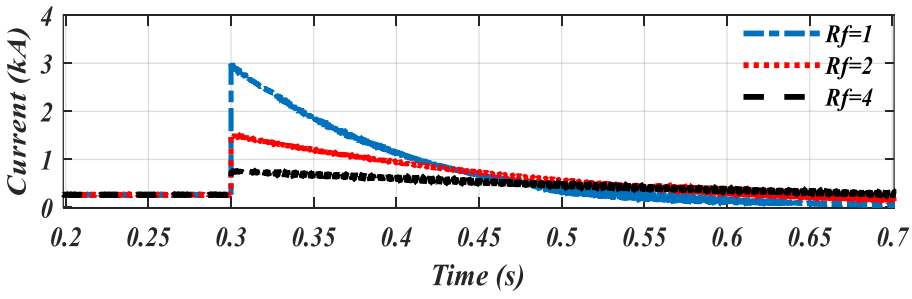
(b)



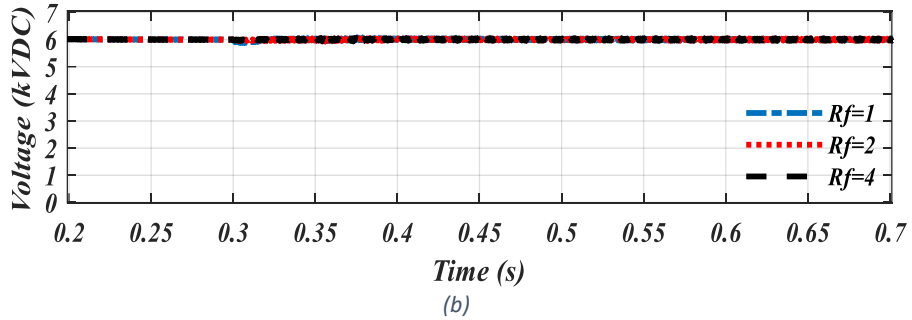
(c)

Figure 4.10: Pole-to-ground high grounding impedance 6 kVDC Fault #1: (a) current in kA (b) DC bus voltage (c) positive and negative pole voltages.

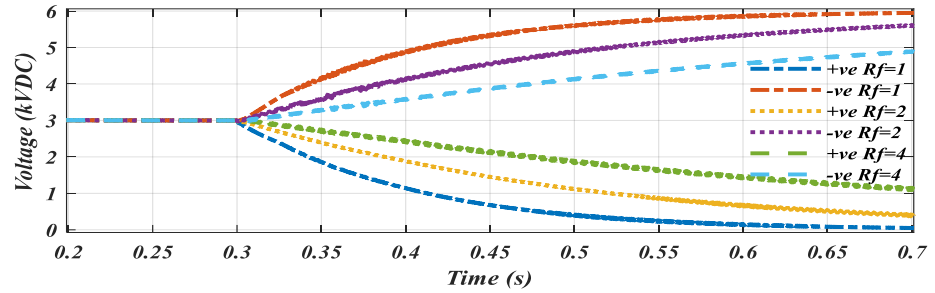
Fig. 4.11 (a), (b), (c) and (d) show the current, bus voltage, pole voltages, and speed of motor M4, respectively. The peak fault current was taken on the feeder line of M1 as shown in Fig. 4.5. Fig. 4.11 (a) shows the fault current of the three different grounding cases, and the first stage fault current peaks are 3 kA, 1.5 kA and 750 A for R_{f1}=1Ω, R_{f2}=2Ω and R_{f3}=4Ω respectively. The DC bus voltages are shown in Fig. 4.11 (b). The motor speeds (M4 here specifically) are shown in Fig. 4.11 (c). If the fault current is less than the rated take-off current, the traditional detection technique is not possible to be used. Further details and discussion will be covered in Chapter 6.



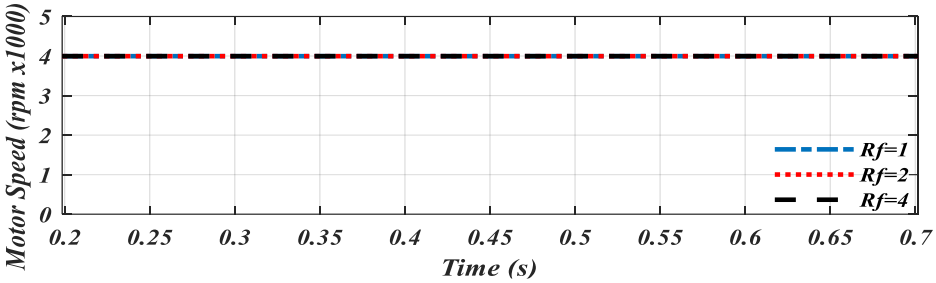
(a)



(b)



(c)



(d)

Figure 4.11: Pole-to-ground high grounding impedance Fault #2: (a) current in kA (b) DC bus voltage (c) positive and negative pole voltages (d) M4 motor speed.

4.4 Case 2 – 9 kV DC-link

Using the same methodology from the 6 kVDC system, all system parameters have been modified to fit the 9 kVDC system. The system parameters of 9 kVDC are shown in Table 4.4. The two voltage levels (6 and 9 kVDC) were chosen based on the 4 to 10 kVDC voltage range recommended by NASA's comprehensive studies [16], [20].

Table 4.4: TeA architecture components for 9 kVDC system.

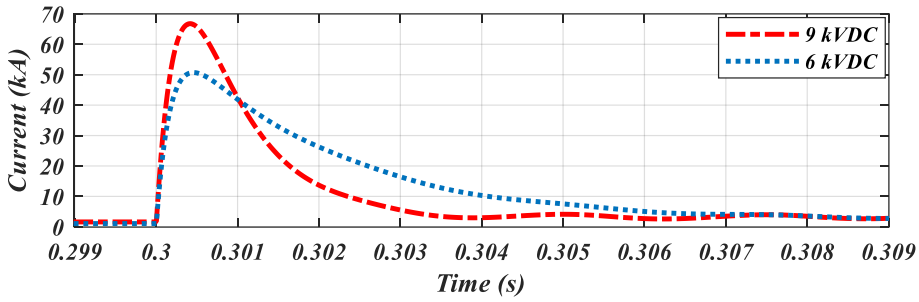
Parameter	Quantity	Value
Generator	1	11.20 MW, 9 kV
Motor	4	2.80 MW ~ rating
		1.5626MW ~ cruise
Converters:		
AC/DC	1	11.20 MW
DC/AC	4	2.80 MW
Cables:		
Transmission	1 (40 m)	XLPE copper, 800 mm^2
		21 mΩ/km,0.503 mH/km
Feeder	4 (5 m)	XLPE copper, 185 mm^2
		90.81 mΩ//km, 0.640 mH/km
DC-link capacitor	2	17.9 mF
Inverter Capacitor	8	1.5 mF

The results of the simulations in the 9 kVDC system will be compared with the results in 6 kVDC system to show the effect of the voltage level, DC-link capacitors, and line impedances on fault behaviours in the next sections.

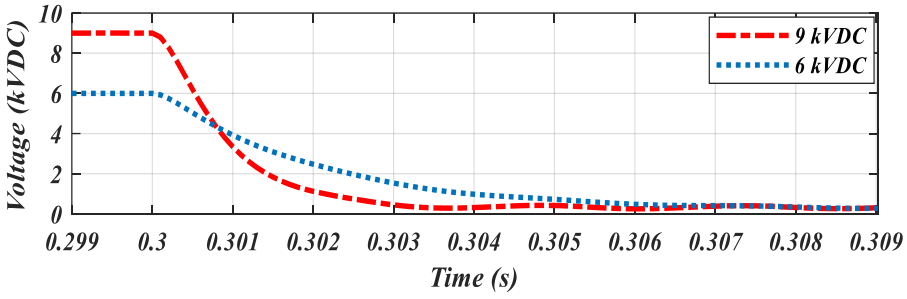
4.4.1 Pole-to-pole fault

Fig. 4.12 (a) compares the fault currents of the 6 kVDC and the 9 kVDC systems when the fault occurs at location Fault #1 at t=0.3 sec. The 9 kVDC system fault reaches

67.48 kA which is 35.1 times the rated current, whereas the 6 kVDC fault was 51.8 kA. The fault current increased by 23.24 % going from 6 to 9 kVDC, despite having higher line impedances and smaller DC-link capacitors. The 9 kVDC system's bus voltage also went down faster than in the 6 kVDC system as shown in Fig. 4.12 (b), mainly due to the smaller capacitor in the 9 kVDC system.



(a)



(b)

Figure 4.12: Comparison between 6 and 9 kVDC Pole-to-pole Fault #1: (a) current in kA (b) DC bus voltage

Fig. 4.13 (a), (b) and (c) show the current, DC bus voltage and speed of motor M4 , respectively, with Fault #2 applied. The fault current of the 9 kVDC has the same patterns of the 6 kVDC for Fault #2. However, the 9 kVDC fault is higher than the 6 kVDC by 26% and 21.16% for the first and second peaks, respectively.

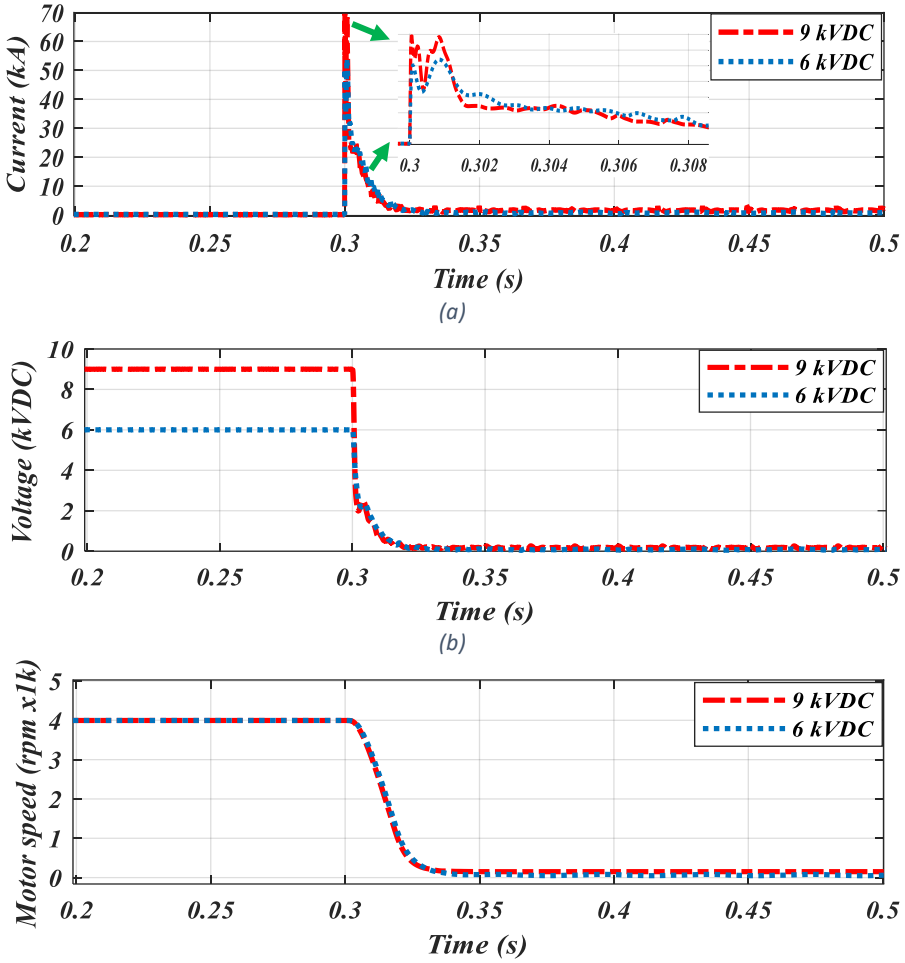


Figure 4.13: Comparison between 6 and 9 kVDC Pole-to-pole Fault #2: (a) current in kA (b) DC bus voltage (c) M4 motor speed.

4.4.2 Pole-to-ground low grounding impedance fault (Metallic)

Fig. 4.14 (a) and (b) compares the fault currents and DC bus voltages of the pole-to-ground fault with low grounding impedance with Fault #1 applied at t=0.3 sec. Like the pole-to-pole fault, the 9 kVDC fault is higher than the 6 kVDC fault by 28%. The recovery time of the 9 kVDC system is faster than for the 6 kVDC one as shown in Fig. 4.14 (b).

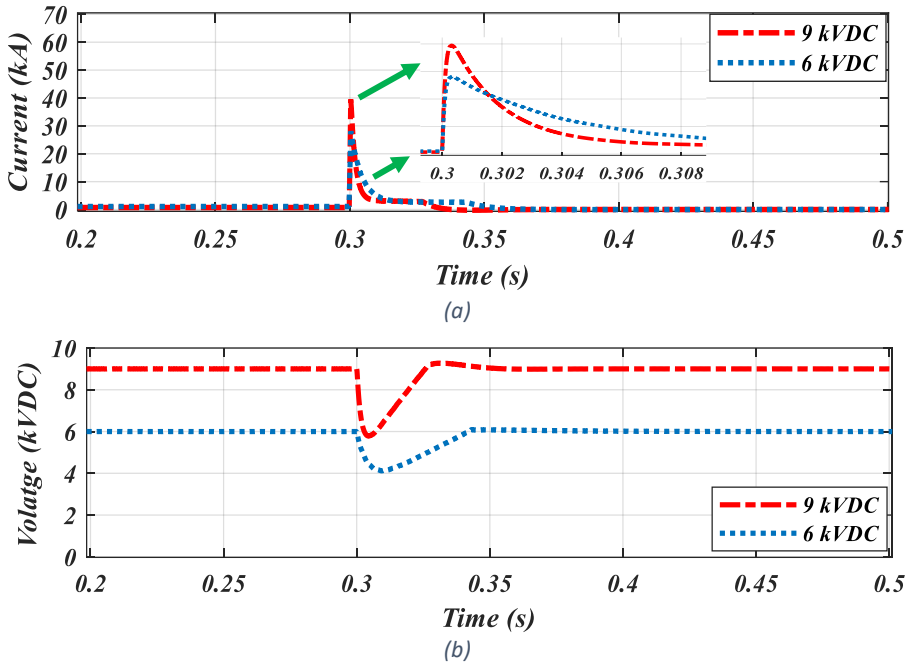


Figure 4.14: Comparison between 6 and 9 kVDC Pole-to-ground low grounding impedance Fault #1: (a) current in kA (b) DC bus voltage

Fig. 4.15 (a), (b) and (c) show the current, DC bus voltage and speed of motor M4, respectively, with Fault #2 applied. The 9 and 6 kVDC systems have the same fault patterns, but the former has higher fault currents. Because of the higher voltage in the 9 kVDC system, the faulty pole's capacitor was discharged faster than in the 6 kVDC system, and the healthy pole's capacitor was also charged faster in the 9 kVDC system. As a result, the 6 kVDC system has a slower recovery time as seen in Fig. 4.15 (b), causing a short drop in motor speed as seen in Fig 4.15 (c).

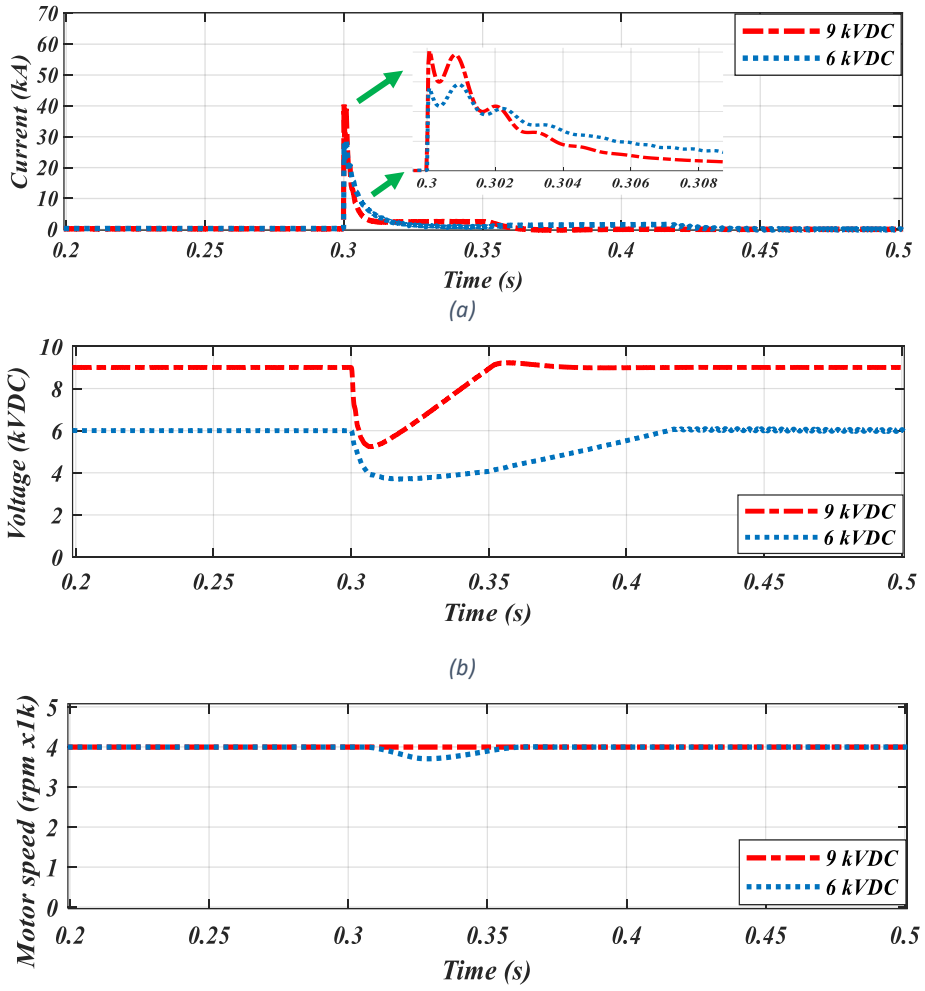


Figure 4.15: Comparison between 6 and 9 kVDC Pole-to-ground low grounding impedance Fault #2: (a) current in kA (b) DC bus voltage (c) M4 motor speed

4.4.3 Pole-to-ground high grounding impedance fault (CFRP)

Fig. 4.16 (a) compares the fault currents of the 9 kVDC system with Fault #1 applied with different high grounding impedances; R_{f1}=1Ω, R_{f2}=2Ω and R_{f3}=3Ω. The fault currents are 4.5 kA, 3 kA and 1.5 kA for R_{f1}=1Ω, R_{f2}=2Ω and R_{f3}=3Ω, respectively. A short intermediate voltage drop appears with R_{f1}=1Ω, whereas the voltage was more stable with R_{f2}=2Ω and R_{f3}=3Ω as shown in Fig. 4.16 (b).

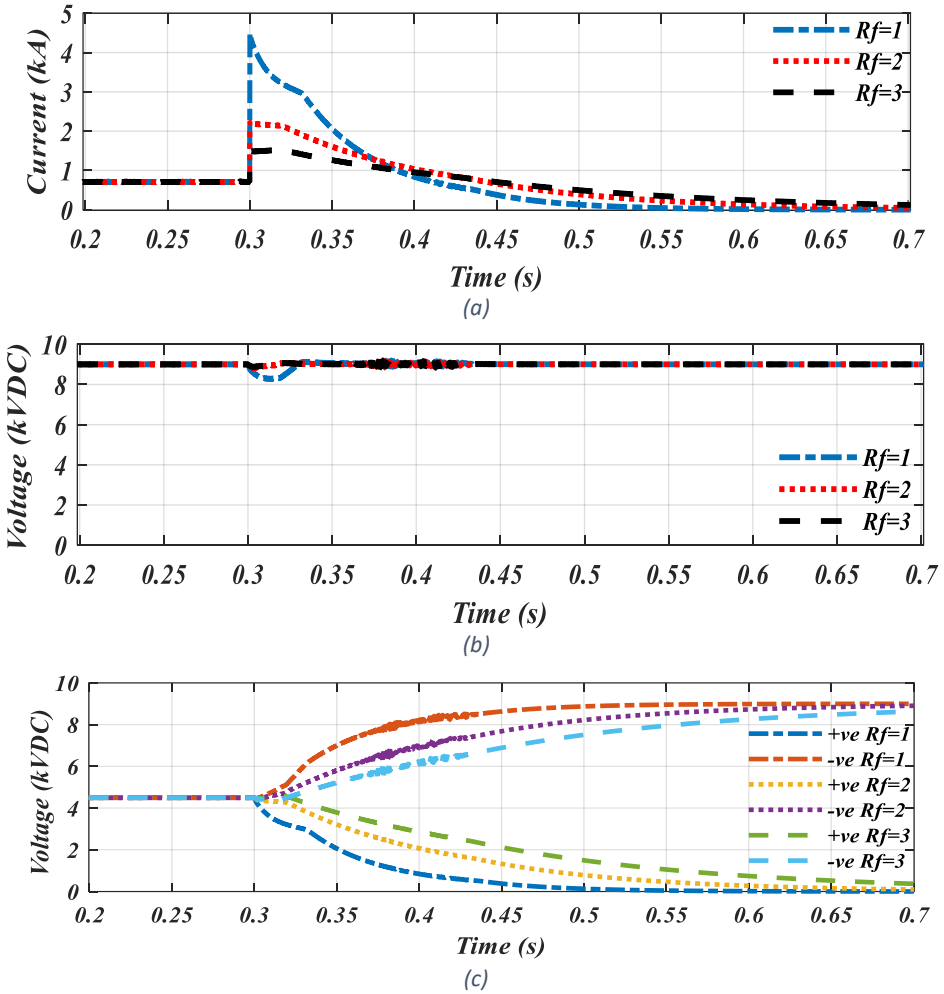


Figure 4.16: Pole-to-ground high grounding impedance Fault #1: (a) current in kA (b) DC bus voltage (c) positive and negative pole voltages

Fig. 4.17 (a) compares the fault currents of the 9 kVDC system with Fault #2 applied with different high grounding impedances; R_{f1}=1Ω, R_{f2}=4Ω and R_{f3}=9Ω. The fault currents are 4.5 kA, 1.125 kA and 500 A, respectively. Again, a short intermediate voltage drop appears with R_{f1}=1Ω, while higher voltage stability was seen with R_{f2}=4Ω and R_{f3}=9Ω as seen in Fig. 4.17 (b). The speeds of the motors on the other feeders weren't affected by the fault in M1's feeder, as seen for M4 in Fig. 4.17 (d).

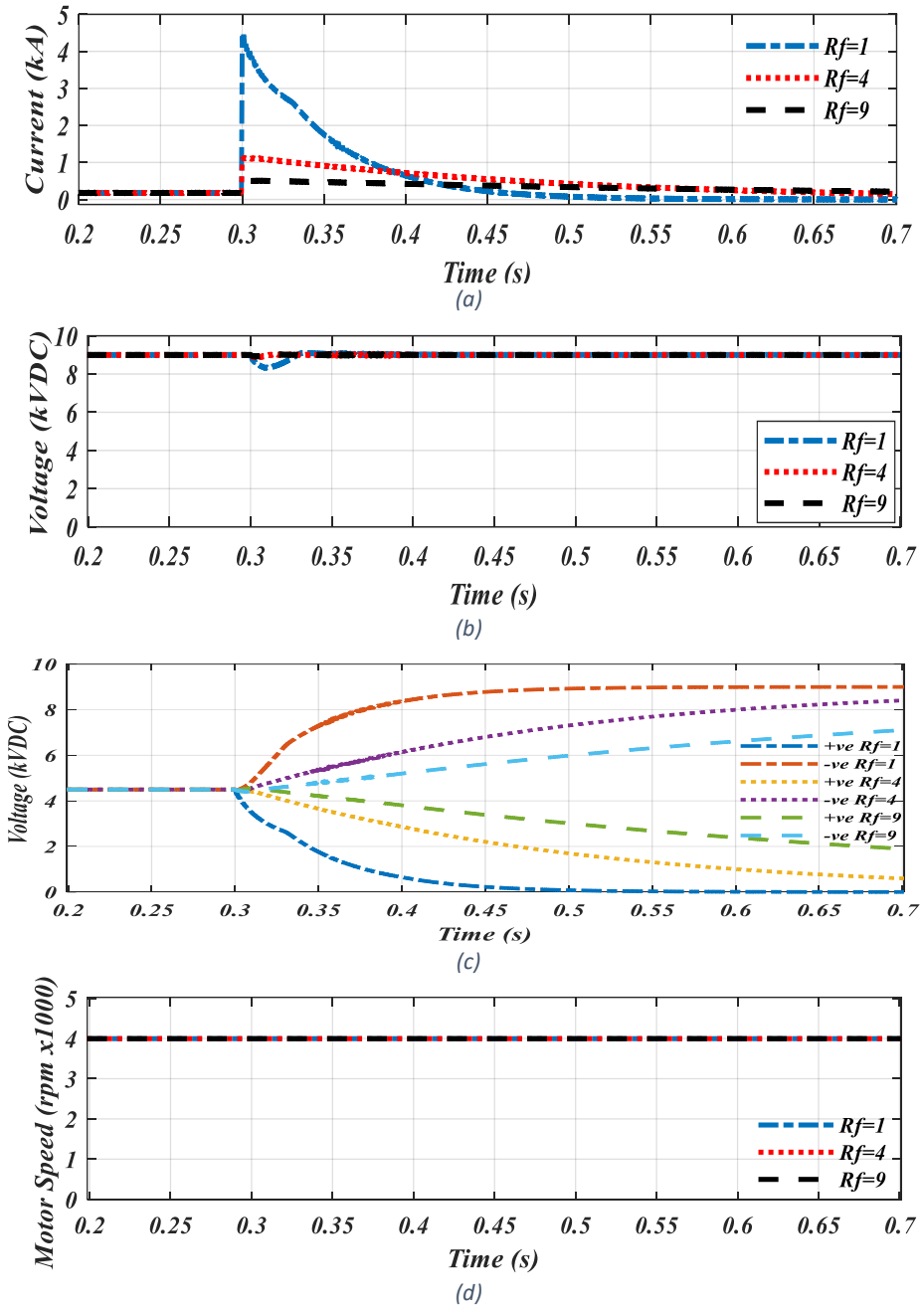


Figure 4.17: Pole-to-ground high grounding impedance Fault #2: (a) current in kA (b) DC bus voltage (c) positive and negative pole voltages (d) M4 motor speed.

4.5 Chapter discussion and conclusions

The DC fault analysis for TeA was done using simulation models in MATLAB®/Simulink and theoretical calculations. The simulation model and the theoretical calculation results show great agreement. The DC fault behaviours depend mainly on four factors, the voltage level, DC-link capacitors, line impedance and grounding impedance.

In order to compare the effect of the four factors on the fault behaviours in TeA, two TeA electrical systems with different voltage levels were compared; 6 kVDC and 9 kVDC, each having different DC-link capacitors and line impedances. The results show that the faults are higher in the 9 kVDC system than in the 6 kVDC system, despite the smaller DC-link capacitors and higher line impedances in the 9 kVDC system.

Because the grounding impedance depends mainly on the material of the airframe (aluminium alloy/CFRP), the pole-to-ground faults were carried out with aluminium alloy grounding for the low grounding impedance cases and with CFRP grounding for the high grounding impedance cases. With low grounding impedances, the fault is extremely high, thus designing an appropriate protection system is a challenge due to the need for high current protection. However, with high grounding impedances, the main challenge is fault detection. In Chapter 5, SFCLs are designed/modelled and integrated to the TeA's power system architecture to limit the extreme high fault current. Chapter 6 shows the detection techniques and the effect of the SFCLs on the protection system and detection methods.

The DC fault analysis in this chapter is based on simulation models and numerical equations in the MATLAB®/Simulink environment. Simulation models are an important step in having a clear vision for system behaviours during unexpected faults and designing a protection system. Part of the future work is to build a DC test rig that simulates the predicted faults to test the protection devices proposed in the following chapters (the SFCL) via experiments. This step is discussed further in the future work section.

Chapter Five

5. Design of a Multilayer Thermoelectric SFCL for Turboelectric Aircraft

5.1 Introduction

Chapter 4 presented and analysed the extreme fault behaviours in TeA power system architecture for pole-to-pole and pole-to-ground low grounding impedance faults due to the compact nature of the DC system network, relatively high voltage level and low line impedance. In this chapter, the importance of SFCL for TeA is discussed, whereby multilayer thermoelectric SFCLs are modelled and integrated for the DC transmission and feeder lines in TeA. This model is an improved version based on the quench behaviour modelling done in [89] and [145]. A multifunctional superconducting device is used to improve the system stability in wind farms [89], while a superconducting cable is designed for electric aircraft in [145]. Both studies consider two layers of the superconductor tape, which are the superconductor layer (e.g. YBCO) and the stabilizer layer (e.g. copper), and show satisfactory results. The model presented in this thesis considers all superconductor tape layers while determining the electrical and thermal behaviours for each layer, and the current is shared between the layers based on the current divider rule. The focus of the SFCL's design is not only on the fault limiting capability but also on the recovery time under load conditions. The impact of different copper stabilizers and shunt resistors on SFCLs is demonstrated. Finally, SFCLs are tested under different fault locations to show the effectiveness/importance of SFCL in TeA power system architecture.

5.2 The importance of SFCL in TeA power system

The importance of the SFCL in TeA comes from the fact that the rise time and the magnitude of the pole-to-pole and pole-to-ground low grounding impedance faults are extremely high, while the fastest DCCB is still relatively slow (around 4 msec) [73]. In the TeA 6 kVDC, the magnitude of the pole-to-pole fault is 51.8 kA and reaches the peak time at t= 0.45 msec. By using Eq. 4.14, Fig. 5.3 shows the peak value of the current faults against some of the low grounding impedances.

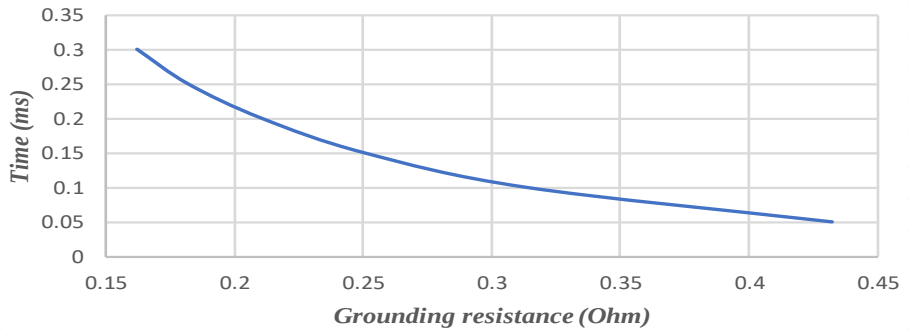


Figure 5.1: Peak time of the fault vs. grounding impedance.

The results of Fig. 5.1 and the pole-to-pole fault magnitude and rise time demonstrate a real need for SFCLs in TeA as the SFCL can handle the fault immediately, thereby reducing the fault current and ensuring that the CBs operate safely.

5.3 Multilayer thermoelectric superconducting fault current limiter model in MATLAB/Simulink

An SFCL is a self-acting electrical device that reduces the magnitude of current during a fault to allow the protection devices (e.g. circuit breakers) within a network to operate without extremely high electrical stresses. SFCLs usually operate within very short time, depending on the fault magnitude and rise time. When the current magnitude exceeds the critical current of the SFCL, the resistivity of the SFCL increases sharply, reducing the fault current magnitude [90], [146].

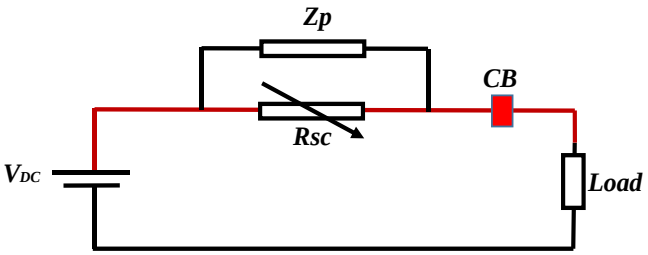


Figure 5.2: Electric circuit of a resistive SFCL with parallel impedance.

As the TeA has a compact electrical network operating at relatively high voltages, faults are guaranteed to cause very high currents to flow through the electrical grid, thereby very likely exceeding the maximum ratings of the protection systems (CBs or switchgears). This might even cause permanent damage to normally operating devices like IGBTs, diodes, motors, cables, etc. As such, the use of an SFCL is necessary to avoid these electrical stresses and allow the CBs to operate safely.

There are two main types of SFCLs: resistive and inductive SFCLs (r-SFCLs and i-SFCLs, respectively). r-SFCLs are lighter and have simpler designs [90], [147] and are especially helpful as weight reduction is crucial in designing TeA. Thus, an r-SFCL is used in this study, with the traditional circuit shown in Fig. 5.2. The two most common superconductors used for SFCLs are YBCO and BSCCO, both of which are HTS. In this study, YBCO is used as it offers better performance [105], [148].

The behaviour of an r-SFCL is controlled by the superconductor tapes, which are used to construct the r-SFCL. In this study, YBCO wires (SCS12050, manufactured by *SuperPower Inc.*) [149] cooled by LN_2 (77 K) are used to construct the r-SFCL device. The sizes and materials of the superconductor tape layers are shown in Fig. 5.3.

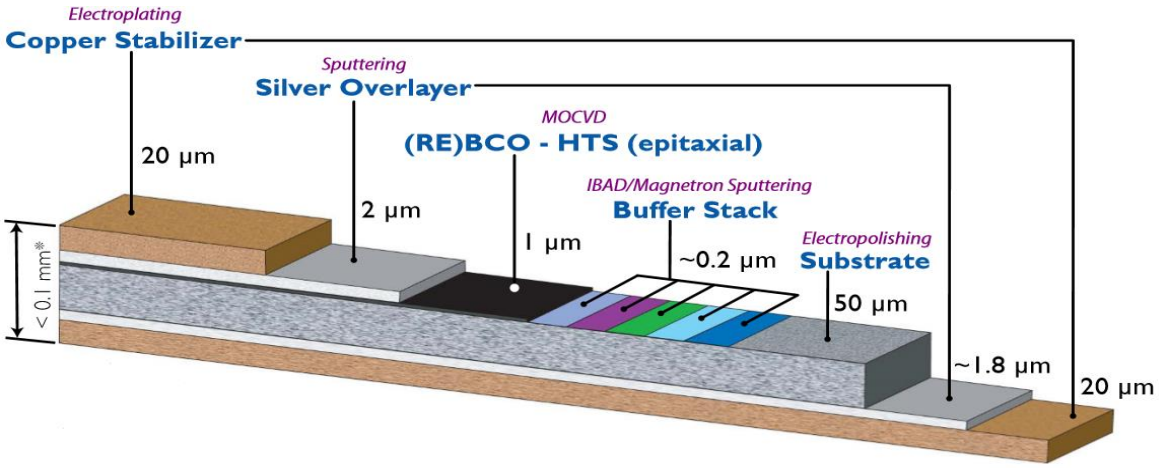


Figure 5.3: Superconductor materials (SCS12050).

The behaviour of the superconductor tape in the r-SFCL is mainly controlled by its critical temperature and critical current density. When the current is less than the critical current of the superconductor tape and the temperature of the superconductor tape is less than the critical temperature of the r-SFCL (93 K), the tape works in a superconductive state, and the current passes through the YBCO layer, i.e., its resistivity is almost zero ($\rho_{sc} \approx 0$). However, when the critical current is exceeded, the resistivity of the YBCO layer increases sharply, and the current redirects to the other layers of the tape (mainly the copper stabilizer). The electric representation of the tape is shown in Fig. 5.4.

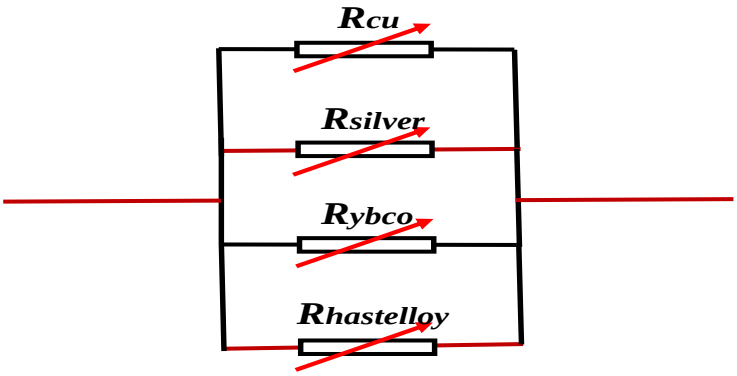


Figure 5.4: Electric representation of SCS12050 tape.

The resistivity of the YBCO layer can be calculated by Eq. 5.1:

$$\rho_{YBCO} = \frac{E_c}{J_c(T)}\left(\frac{J}{J_c(T)}\right)^{N-1} \qquad T < T_c\ ,\ J > J_C \tag{5.1}$$

Where E_c = 1 μV/cm, which is the standard electrical field used for superconductors. For the YBCO tapes, the N value ranges between 21 and 30 [150]. Eq. 5.1 is only valid when the temperature is less than the critical temperature, which is 93 K for YBCO, and the current density is higher than the critical current density (i.e., $J > J_C$). The critical current density is dependent on the temperature and can be calculated by Eq. 5.2:

$$J_c(T) = J_{co}\left(\frac{(T_c - T(t))^a}{(T_c - T_o)^a}\right) \qquad T_o < T < T_c \tag{5.2}$$

Where J_{co} is the critical current density at the initial temperature T_o, which equals 77 K, the boiling point temperature of liquid nitrogen (LN_2, the coolant in this study), α is the density exponent and equal to 1.5 [96], and Tc is the critical temperature; Eq. 5.2 is only valid for $T_o < T < T_c$.

Under these two conditions, the YBCO tape's resistivity is equal to that of the superconducting layer ($\rho_{sc} \approx \rho_{HTS}$). However, when the temperature exceeds the critical temperature, the resistivity of the YBCO layer exceeds that of the other layers, redirecting most of the current through the different layers, mainly the copper layers. The resistivity of the copper and silver layers is temperature-dependent and can be calculated by Eqs. 5.3 and 5.4, respectively.

$$\rho_{cu} = (0.0084 \times T - 0.4603) \times 10^{-8} \tag{5.3}$$

$$\rho_{Ag} = 0.285 \times 10^{-8}[1 + \alpha(T - T_o)] \tag{5.4}$$

Where T_o is LN_2 boiling temperature (77 K) and α is the temperature coefficient and equal to 0.0038 per Kelvin degree. The temperature-dependent resistivity of the Hastelloy substrate is shown in Fig. 5.5.

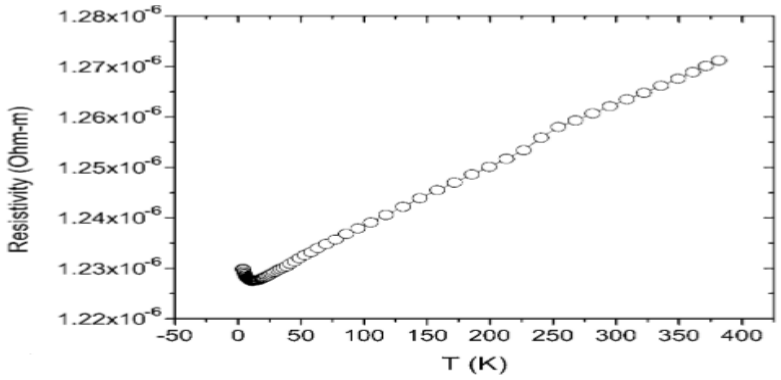


Figure 5.5: The resistivity of Hastelloy vs. temperature [151].

Based on Fig. 5.5, the resistivity of the Hastelloy can be calculated by Eq. 5.5:

$$\rho_{Hast.} = (1.333 \times 10^{-10})T + 1.216 \times 10^{-6} \tag{5.5}$$

The resistance of the superconducting tape can be obtained by Eq. 5.6:

$$\frac{1}{R_{sc}} = \frac{1}{R_{YBCO}} + \frac{1}{R_{cu}} + \frac{1}{R_{Ag}} + \frac{1}{R_{Hastelloy}} \tag{5.6}$$

Where:

$$R_{YBCO} = \rho_{YBCO} \frac{l}{A_{YBCO}} \tag{5.7}$$

$$R_{cu} = \rho_{cu} \frac{l}{A_{cu}} \tag{5.8}$$

$$R_{Ag} = \rho_{Ag} \frac{l}{A_{Ag}} \tag{5.9}$$

$$R_{Hast.} = \rho_{Hast.} \frac{l}{A_{Hast.}} \tag{5.10}$$

Where l and A are the lengths and cross-sectional areas of each layer.

Eqs. 5.1 to 5.10 calculate the electrical resistance of the superconductor layers. However, the electrical resistivities of the layers are temperature-dependent; therefore, to get an accurate value for the r-SFCL, the thermal part of the r-SFCL must be

calculated accurately. The temperature of the superconductor tape is obtained by Eq. 5.11:

$$T(t) = T_o + \frac{1}{C_p}\int_0^t Q_{sc}(t)dt \tag{5.11}$$

Where Q_{sc} corresponds to the net power in the tape and can be calculated by Eq. 5.12. and C_p is the heat capacity of the layer materials. T_o is the initial temperature, which equals 77 K.

$$Q_{sc}(t) = P_{diss}(t) - P_{cooling}(t) \tag{5.12}$$

Where $P_{diss}(t)$ represents the dissipated power in the superconducting tape and $P_{cooling}(t)$ is the cooling power representing the energy absorbed by the cooler. $P_{cooling}(t)$ reduces the temperature rise during a fault and returns the tape to a superconductive state after the fault is cleared. $P_{diss}(t)$ and $P_{cooling}(t)$ are calculated by Eqs 5.13 and 5.14, respectively:

$$P_{diss}(t) = i(t)^2 R_{sc}(t) \tag{5.13}$$

$$P_{cooling}(t) = hA(T(t) - T_o) \tag{5.14}$$

Where A is the surface area of the SFCL, which is covered by the LN_2 coolant. In this model, 100% of the r-SFCL is exposed to the coolant. There are several ways to design a 100% exposed area of the r-SFCL; these are presented in the following papers [152], [153] and are shown in Fig. 5.6.

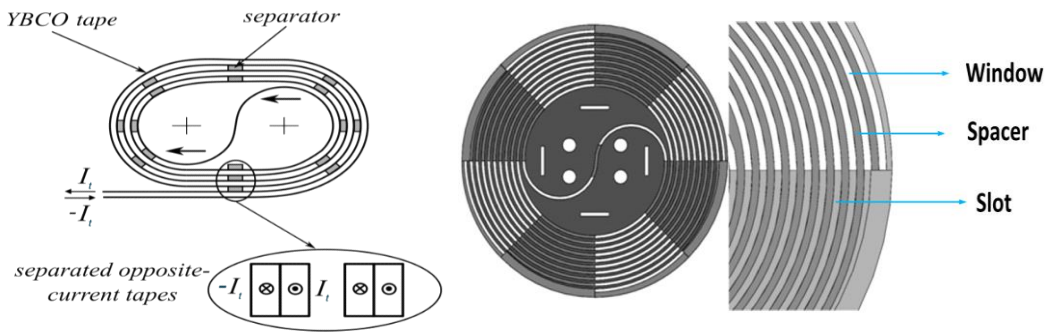


Figure 5.6: SFCL construction; whole area of the superconductor tape exposed to the LN2 [152][153].

h is the heat transfer coefficient, which mainly depends on the temperature difference ΔT between the outer surface of the tape and the coolant LN_2, pressure and heat capacity. The heat transfer coefficient h behaves in a nonlinear way and also has two different behaviours in heating and cooling processes. In the heating process, the behaviours of the h coefficient can be divided into three different stages, as shown in Fig. 5.7 [154]: free convection, bubble boiling and film boiling. In the bubble boiling stage, the h coefficient increases sharply; therefore, the heat transfer process increases. As a result, the superconductor tape quenches faster. However, during the cooling process, the h coefficient curve rises gradually. As a result, the recovery time stage takes a longer time. In this study, the h coefficient curve of Fig. 5.7 has been adopted to characterise the behaviour of the h coefficient during heating and cooling processes [154], [155].

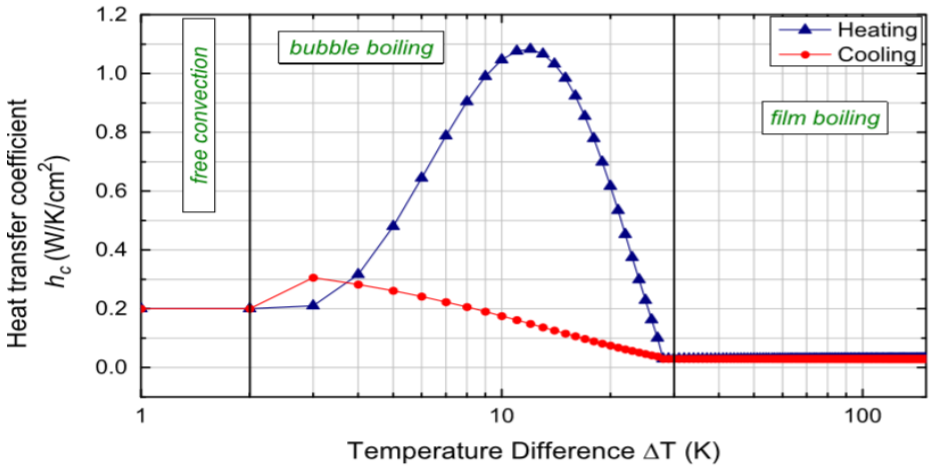


Figure 5.7: Heat transfer coefficient curve between the surfaces of the HTS tapes and LN_2 at room pressure [93].

Cp is the heat capacity (J/K) of the superconducting tape. The Cp of the tape is determined by the heat capacity of each layer in the tape. The superconducting tape in this study consists of YBCO, Hastelloy substrate, copper and silver layers, as shown in Fig. 5.3. The buffer stack size is only 0.2 µm, which represents only 0.2% of the tape;

thus, the buffer stack layer is negligible and ignored in this study. The Cp of the superconductor tape can be calculated by Eq. 5.14:

$$Cp = Cpybco + CpHast + Cpcu + CpAg \quad (5.14)$$

Based on the data in [156], the heat capacity of the YBCO layer is approximated by the linear Eq. 5.15:

$$C_{pybco} = 2T\ d_{ybco}\ V_{ybco} \quad (5.15)$$

Where T, d_{ybco} and V_{ybco} are the temperature, density and volume of the YBCO layer.

The specific heat capacity of the Hastelloy layer is shown in Fig. 5.8, based on the [151]:

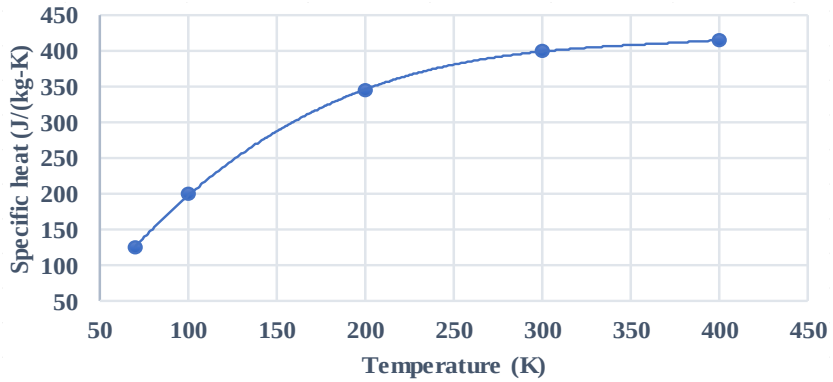


Figure 5.8: Specific heat capacity of Hastelloy w.r.t temperature 77 to 400 K.

Based on the data in Fig. 5.9, the specific heat capacity and the heat capacity of the hastelloy layer is calculated by Eq. 5.16 and Eq. 5.17, respectively:

$$C_{Hast.} = 9.8 \times 10^{-6}\ T^3 - 0.01062\ T^2 + 3.987T - 104.21 \quad (5.16)$$

$$C_{pHast.} = C_{Hast.}\ d_{Hast.}\ V_{Hast.} \quad (5.17)$$

Where T, d_{Hast}, V_{Hast} are the temperature, density and volume of the Hastelloy layer.

The specific heat capacity of the copper layer is shown in Fig. 5.9 [157]:

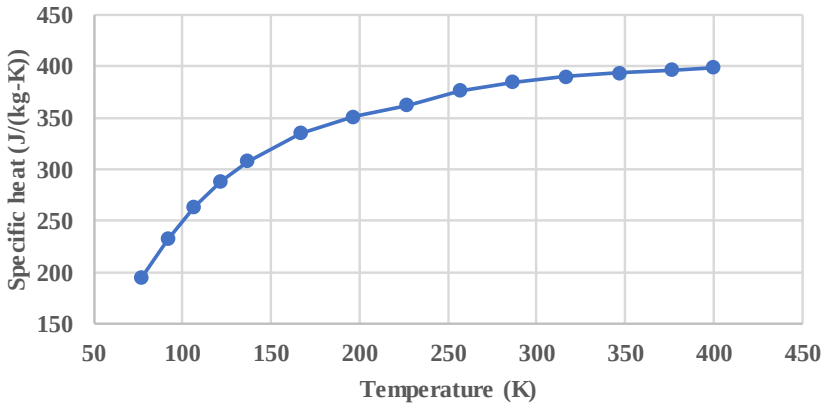


Figure 5.9: Variation of the specific heat of copper w.r.t. temperature from 77 to 400 K.

The specific heat capacity and the heat capacity of the copper layer are calculated by Eq. 5.17 and Eq.5.18, respectively:

$$C_{cu} = 1.27 \times 10^{-5}T^3 - 0.0119T^2 + 3.775T - 24.32 \quad (5.17)$$

$$C_{pcu} = C_{cu} d_{cu} V_{cu} \quad (5.18)$$

Where C_{cu}, d_{cu}, V_{cu} are the specific heat capacity, density and volume of the copper layer.

The specific heat of the silver layer vs. temperature is shown in Fig. 5.10, based on the data in [158]:

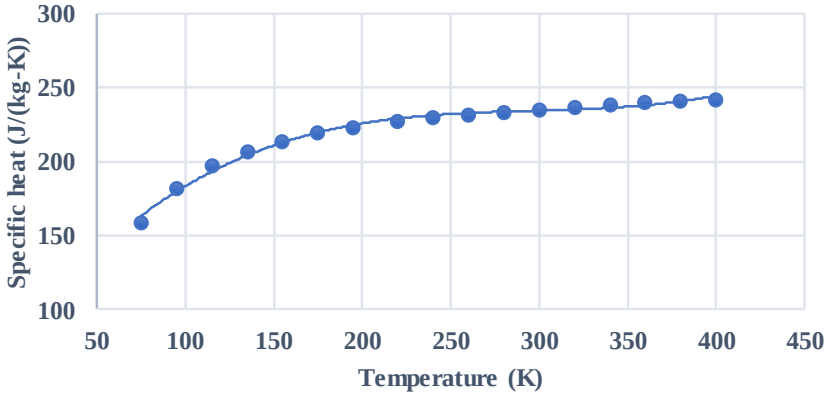


Figure 5.10: Variation of the specific heat of silver w.r.t temperature from 77 to 400 K.

Based on the data in Fig. 5.10, the specific heat capacity and heat capacity of the silver layer are calculated by Eq. 5.19 and Eq. 5.20, respectively:

$$C_{pAg} = 5.8 \times 10^{-6}\, T^3 - 0.005189\, T^2 + 1.5729T + 72.182 \quad (5.19)$$

$$C_{pAg} = C_{Ag} d_{Ag}\, V_{Ag} \quad (5.20)$$

Where C_{Ag}, d_{Ag}, V_{Ag} are the specific heat capacity, density and volume of the silver layer.

The densities of the superconductor materials are shown in Table 5.1:

Table 5.1: Densities of tape materials.

Material	Density (kg/m^3)
YBCO	5,900
Copper	8,940
Hastelloy	8,910
Silver	10,490

Where the volume of each material can be calculated by Eq. 5.21:

$$Volume = Lengt \times Thickness \times Width \times \#\ of\ wires\ in\ parallel \quad (5.21)$$

The behaviour of the superconducting tape can be described by the relationship between the applied current I vs. the critical current I_C and the actual temperature T vs. the critical temperature T_C of the tape. The superconducting tape works in four different states, and all are shown in Fig. 5.12:

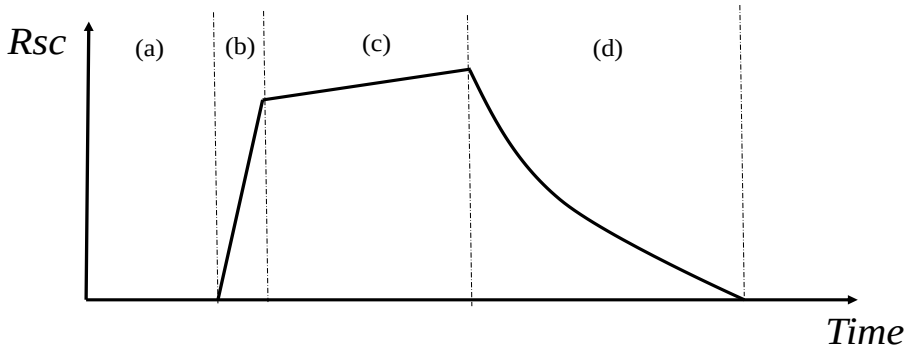


Figure 5.11: Operation modes of superconductor tape; (a) superconducting state, (b) flux-flow state, (c) normal resistance state, (d) recovery state.

(a) $I < I_C \ and \ T < T_C$ (Superconductive State)

When the applied current I in the r-SFCL is less than the critical current Ic of the r-SFCL and the temperature T of the r-SFCL is less than the critical temperature T_C of the r-SFCL, the r-SFCL works in the superconductive state, and the resistivity of the tape approximately equals zero ($\rho sc = 0$).

(b) $I > Ic \ and \ T < T_C$ (Flux-Flow State)

When a fault occurs, the current increases sharply and exceeds the critical current *Ic*. As a result, the YBCO layer quenches, and the resistance of the YBCO layer increases according to Eqs. 5.1 and 5.7. When the resistance of the YBCO layer became equal to or higher than the resistance of the other layers (mainly the copper stabilizer layer R_{cu}), the current starts to be shared between the YBCO and different layers.

(c) $I > Ic \ and \ T > T_C$ (Normal State)

When the applied current I is higher than the critical current Ic and the temperature of superconductor tape T is higher than the critical temperature T_C, the superconductor tape converts from the flux-flow state to the normal state. The current passes through other layers, mainly the copper stabilizer because it has the lowest resistance in the superconductor tape. The resistivity of the copper stabilizer can be calculated as in Eqs. 5.3 and 5.8. It is noticeable that the resistivity of the copper is directly proportional to the temperature.

(d) $I < Ic \ and \ T > T_C$ (Recovery State)

When the fault current is cleared, the superconductor tape returns to a superconducting state, unless it is permanently damaged, which occurs if SFCL temperature exceeds a permanently damaging temperature (400 K) [159]. Because it is assumed that the LN_2 fully covers the whole r-SFCL device, the LN_2 starts to remove the heat that was

generated by the overcurrent, per Eq. 5.11. Several parameters determine the recovery stage period, including the coolant material (LN_2 in this study), cooling technique, exposed area of the SFCL to the coolant, and heat transfer coefficient between the coolant and the SFCL device.

5.3.1 SFCL model in MATLAB/Simulink for a transmission line in TeA

Based on the fault analysis in Chapter 4, the multilayer thermoelectric method is used to model the r-SFCL in TeA to reduce the fault current with three different copper stabilizers. The SCS12050 manufactured by *SuperPower Inc.* with a 40 µm copper stabilizer [149] is used as a standard to simulate the r-SFCL in the TeA. The performance of the SCS 12050 with a 40 µm copper stabilizer is compared to that for the same tape but with 20 and 10 µm copper stabilizers. The parameters of superconductors with 40, 20 and 10 µm copper stabilizers are shown in Table 5.2.

Table 5.2: The design parameters of the r-SFCLs for the transmission line.

Parameter	Value
Critical current (A, single tape)	300
Width (mm)	12
Total thickness (µm)	100/80/70
Copper stabilizer thickness(µm)	40/20/10
Hastelloy stabilizer thickness(µm)	50
YBCO layer thickness (µm)	1
Silver layer thickness (µm)	3.8
Length of tape (m)	420
Rated voltage (kV)	6
Resistance (Ω) @100 K per tape	2.96/5.35/8.96
Resistance (Ω) @300 K per tape	12.94/20.2/28.064
Number of wires in parallel	12
Total resistance (Ω) @100 K	0.262/0.445/0.747
Total resistance (Ω) @300 K	1.077/1.682/2.337

The critical current of a single tape is determined by the datasheet of the superconductor tape [149]. The threshold value of the CBs and the critical current of the r-SFCL are calculated by Eqs. 5.22 and 5.23:

$$CB_{threshold} = (I_{rate-takeoff} + I_{loss}) \times 1.5 \quad (5.22)$$

$$SFCL_{I_{critical}} = (CB_{threshold}) \times 1.2 \quad (5.23)$$

Based on Eqs. 5.22 and 5.23, the critical current of the r-SFCL is calculated as 3.6 kA @ 77 K. The 3.6 kA critical current is achieved by 12 superconductor tapes connected in parallel. The safety margin between the rated current and the threshold point of the CBs is chosen to prevent false operation of the CBs. The safety margin between the critical current of the r-SFCL and the threshold value of the CBs is chosen to allow the detection system to detect the fault current. The power system architecture of the TeA integrated with the r-SFCL in the transmission line is shown in Fig. 5.12.

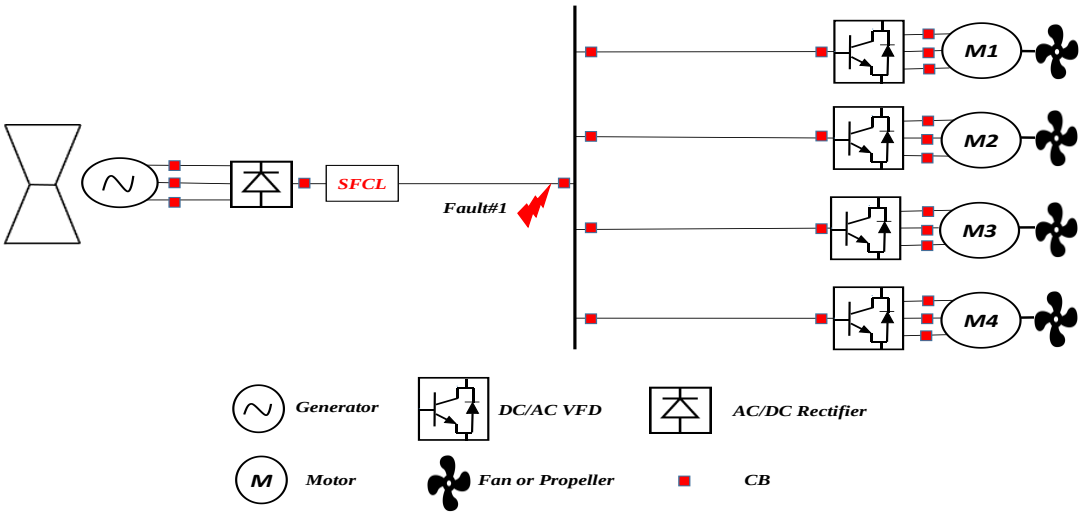


Figure 5.12: TeA power system architecture integrated with SFCL in the transmission line.

In order to test and compare the three different r-SFCLs in the transmission line, the system is subjected to the same 6 kVDC pole-to-pole fault as in Chapter 4 at t=0.3 sec for 20 msec to show the fault current limiting capability and the recovery time behaviour of the three different r-SFCLs. Fig. 5.13 (a) compares the fault current of Fault#1 without r-SFCL with that of the three r-SFCLs with 40, 20 and 10 µm copper stabilizers.

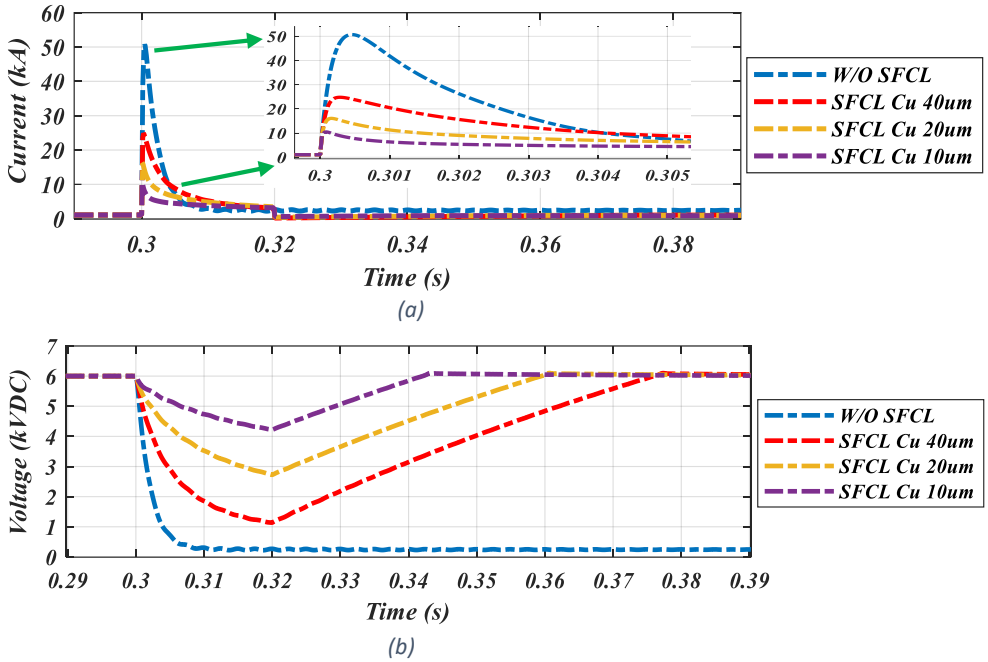


Figure 5.13: System responses with r-SFCLs with different copper stabilizers; (a) current and (b) voltage.

Fig. 5.13 (b) shows the voltage drop of the DC-link without r-SFCL and with the r-SFCL 40, 20 and 10 µm copper stabilizers. Both Figs. 5.13 (a) and (b) show that the fault current and voltage drop are smaller when the r-SFCL copper stabilizer is smaller. When the copper stabilizer is 40 µm (the dot-dashed red line), the first peak of the fault current was 25 kA (50% of the prospective current), and the voltage dropped to almost 1 kV within 20 msec. However, with the r-SFCL 10 µm copper stabilizer (the dot-dashed purple line), the first peak of the fault current was just above 10 kA (20% of the prospective current), and the voltage dropped to almost 4.1 kV after 20 msec. The electrical performance shows that the r-SFCL with the 10 µm copper stabilizer has the highest fault current limiting capability, while the 40 µm shows the lowest fault current limiting capability. However, as the electrical performance is essential for designing the r-SFCL, the recovery time under load conditions and the thermal behaviour have the same importance for system performance.

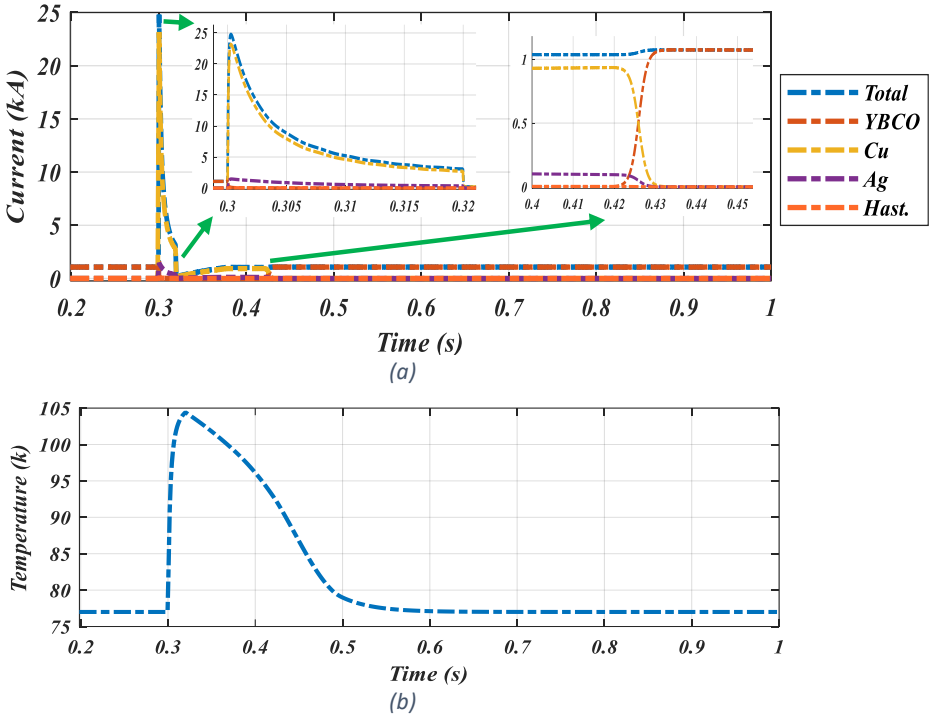


Figure 5.14: SFCL 40 µm copper stabilizer; (a) current passing through each layers and (b) SFCL temperature.

Fig. 5.14 (a) shows the passing currents through each layer of the r-SFCL with a 40 µm copper stabilizer and the recovery time of the r-SFCL. Fig 5.14 (b) shows the temperature of the r-SFCL. The left zoomed figure in Fig. 5.14 (a) shows that the current passed through the YBCO layer (the red dot-dashed line) before the occurrence of the fault. When the fault occurred at t=0.3 sec, the resistance of the YBCO layer increased and the current started to move to the easier paths (layers) with less resistance (copper and silver layers). Most of the current went through the copper layer, as shown by the orange dot-dashed line, because it has the lowest resistance. Less current passed through the silver layer because it has a higher resistance than the copper layer. The Hastelloy layer has the highest resistance, and just a few ampers could pass through it. Fig 5.14 (b) shows that the temperature of the r-SFCL reached 105 K at t=0.32 sec. At t=0.42 sec, the temperature dropped to below 93 K. As a result, the r-SFCL recovered to the superconducting state. The r-SFCL needed 100 msec to recover from the fault. When the temperature dropped to below 93 K, the r-SFCL returned to the superconducting

state. As a result, the current went back to the YBCO layer. as shown in the right zoomed figure in Fig. 5.14 (a).

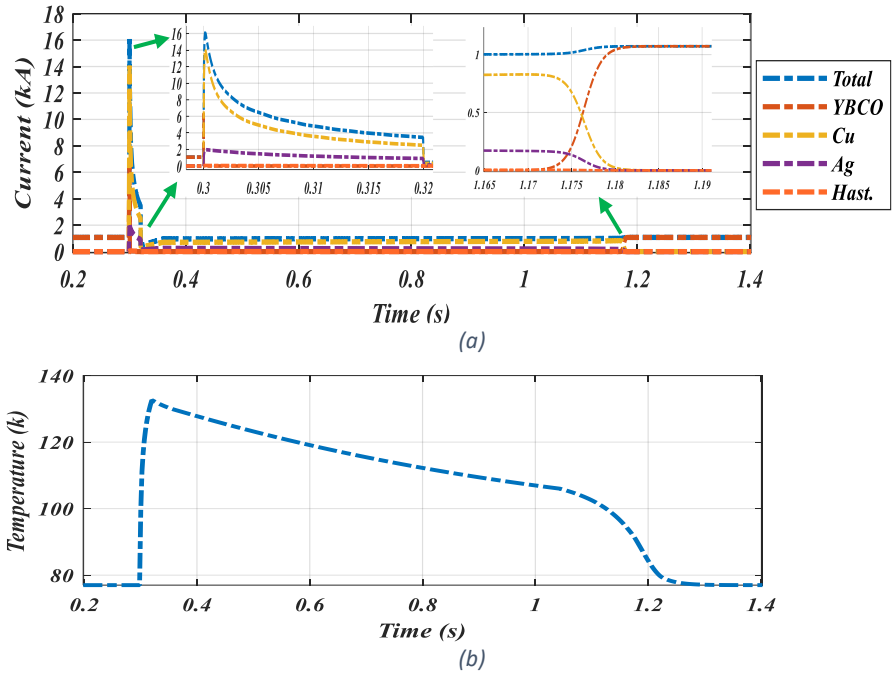


Figure 5.15: SFCL with 20 µm copper stabilizer; (a) current passing through each layer and (b) SFCL temperature.

Fig. 5.15 (a) shows the current passing through each layer of the r-SFCL with the 20 µm copper stabilizer and the recovery time of the r-SFCL. Fig 5.15 (b) shows the temperature of the r-SFCL device. The first peak of the fault was limited to 16 kA (32% of the prospective current). The behaviour of the r-SFCL with 20 µm has the same pattern of the r-SFCL with 40 µm, but with two main differences. Regarding the first one, because the 20 µm copper stabilizer has a higher resistance than the 40 µm copper stabilizer, the passing current through the 20 µm copper stabilizer is less than the passing current with the 40 µm copper stabilizer. In contrast, the current passing through the silver layer with the r-SFCL with the 20 µm copper stabilizer increased compared to the r-SFCL with the 40 µm copper stabilizer. The second difference is that the temperature of the r-SFCL with the 20 µm copper stabilizer increased to 133 K compared to 105 K for the r-SFLC with the 40 µm copper stabilizer. The temperature dropped to less than 93 K at t=1.175 sec and the r-SFCL returned to the superconducting

state, as shown in the right zoomed figure in Fig. 5.15 (a). The r-SFCL needed 855 msec, from 0.32 to 1.175 sec, to recover from the fault.

Fig. 5.16 (a) shows the current passing through each layer of the r-SFCL with the 10 µm copper stabilizer. Fig 5.16 (b) shows the temperature of the r-SFCL. The first peak of the fault was limited to just above 10 kA (20% of the prospective current).

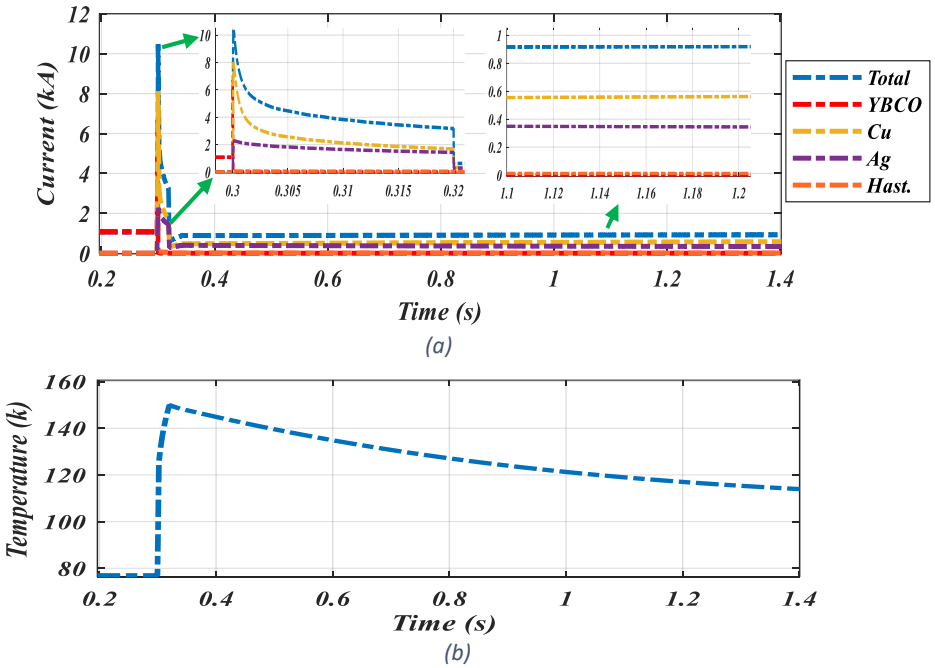


Figure 5.16: SFCL with 10 µm copper stabilizer; (a) current passing through each layer and (b) SFCL temperature.

The highest temperature for the r-SFCL with the 10 µm copper stabilizer was 150 k. In the r-SFCL with the 10 µm copper stabilizer, when the YBCO layer resistance increased, the copper and silver layers started to share more current, as shown by the orange and purple dot-dashed lines in Fig. 5.16 (a). The resistivity of the silver is smaller than the resistivity of the copper. However, the silver layer has a higher resistance than the copper layer because the cross-sectional area of the copper is still higher than the cross-sectional area of the silver (10 µm for copper and 3.8 µm for silver) based on Eqs. 5.8 and 5.9. Based on the results for the r-SFCLs with the 40 and 20 µm copper stabilizers, recovery is possible under load conditions with different copper stabilizers.

However, with the r-SFCL with the 10 µm copper stabilizer, the r-SFCL was not able to recover under load conditions because the heat generated by the r-SFCL was almost equal to the cooling power when the temperature equalled 106 k based on Eqs, 5.11 to 5.15.

The temperatures of the three r-SFCLs with different copper stabilizers are shown in Fig. 5. 17. The first peak of the fault, the highest temperature and the recovery time are shown in Table 5.3.

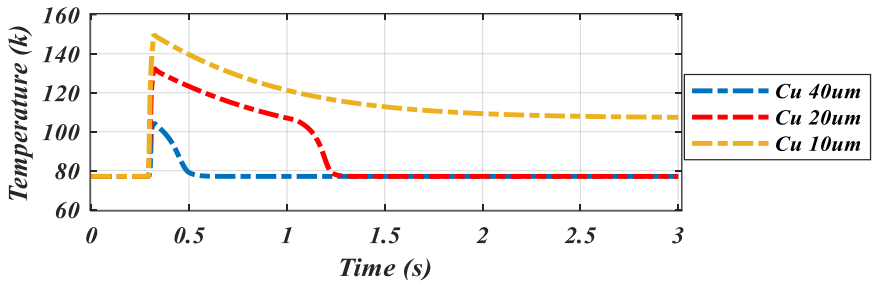


Figure 5.17: Temperatures of the r-SFCLs with the 40, 20 and 10 µm copper stabilizers.

Table 5.3: Comparison of three YBCO r-SFCLs with different copper stabilizers.

TYPE	FIRST PEAK (KA)	HIGHEST TEMP. (K)	RECOVERY TIME (MS)
r-SFCL 40 µm	25	105	100
r-SFCL 20 µm	16	133	855
r-SFCL 10 µm	10	149	Not recovered

Based on Fig. 5.17 and Table 5.3, there is a clear trade-off between the copper stabilizer size, fault current limiting capability, temperature and recovery time. When then copper stabilizer is smaller, the first peak current is smaller. However, the temperature of the r-SFCL is higher and the recovery time is longer if the r-SFCL is able to recover. Before choosing the r-SFCL type for the TeA, in the next subsection, the impact of shunt resistors on the r-SFCL is discussed.

5.3.1.1 The impact of the shunt resistors on r-SFCL performance

The r-SFCL has to be carefully designed to withstand the overcurrent of the fault, which causes a rise in the temperature, which in turn may result in damage to the r-SFCL coils. Adding a parallel resistor (a shunt resistor) to the r-SFCL has several advantages, including reducing the maximum temperature of the r-SFCL and shortening the recovery time of the r-SFCL. Besides, the shunt resistor works as a protection device to protect the r-SFCL from any unexpected increase in temperature, working as an alternative path for the current to avoid more damage to the r-SFCL. However, the shunt resistor value must be carefully chosen to be able to protect the r-SFCL while maintaining a good fault current limiting capability.

Based on the results in the previous section, the r-SFCL with the 40 µm copper stabilizer is not at risk of high temperature. Also, the fault current limiting capability is not good enough. Thus, the r-SFCL with the 40 µm copper stabilizer is not considered in this section. The impact of the shunt resistor on the r-SFCLs with the 20 and 10 µm copper stabilizers are investigated in the next subsections.

5.3.1.1.1 Case study #1 r-SFCL with 20 µm copper stabilizer

In this section, the r-SFCL with the 20 µm copper stabilizer is tested with different shunt resistors. In order to investigate the impact of the shunt resistor on the r-SFCL, the value of the shunt resistor has to be chosen in the range of the r-SFCL resistance value. In this study, the first shunt resistor value is determined based on Eq. 5.24:

$$R_{shunt} = \frac{R\_SFCL_{100k} + R\_SFCL_{300}k}{2} \tag{5.24}$$

In this section, the r-SFCL with three different shunt resistors are compared to obtain the optimal value of the shunt resistor. The first shunt resistor is calculated by Eq. 5.24. to be 1.0635 Ω. The second and third values are determined as 60% and 200%, respectively, of the value of Eq. 5. 24. The three shunt resistors values are 0.638, 1.0635 and 2.127 Ω. The system is subjected to the same fault at the same location (Fault #1) of the TeA to investigate the impact of the shunt resistors. The duration of the fault is 20 msec, from t=0.3 to t=0.32 sec. The fault current limiting capabilities of the r-SFCL without and with the three shunt resistors are compared in Fig. 5.18 (a). Fig. 5.18 (b) compares the voltage drop of the DC-link without and with the three shunt resistors. The temperatures of the four r-SFCLs are compared in Fig. 5.18 (c). The blue dot-dashed line indicates the values for the r-SFCL without the shunt resistor. The red dot-dashed line indicates the values for the r-SFCL with the highest shunt resistor (R=2.127 Ω). The orange dot-dashed line indicates the values for the r-SFCL with the medium shunt resistor (R=1.0635 Ω). The purple dot-dashed line indicates the values for the r-SFCL with the lowest shunt resistor (R=0.638 Ω).

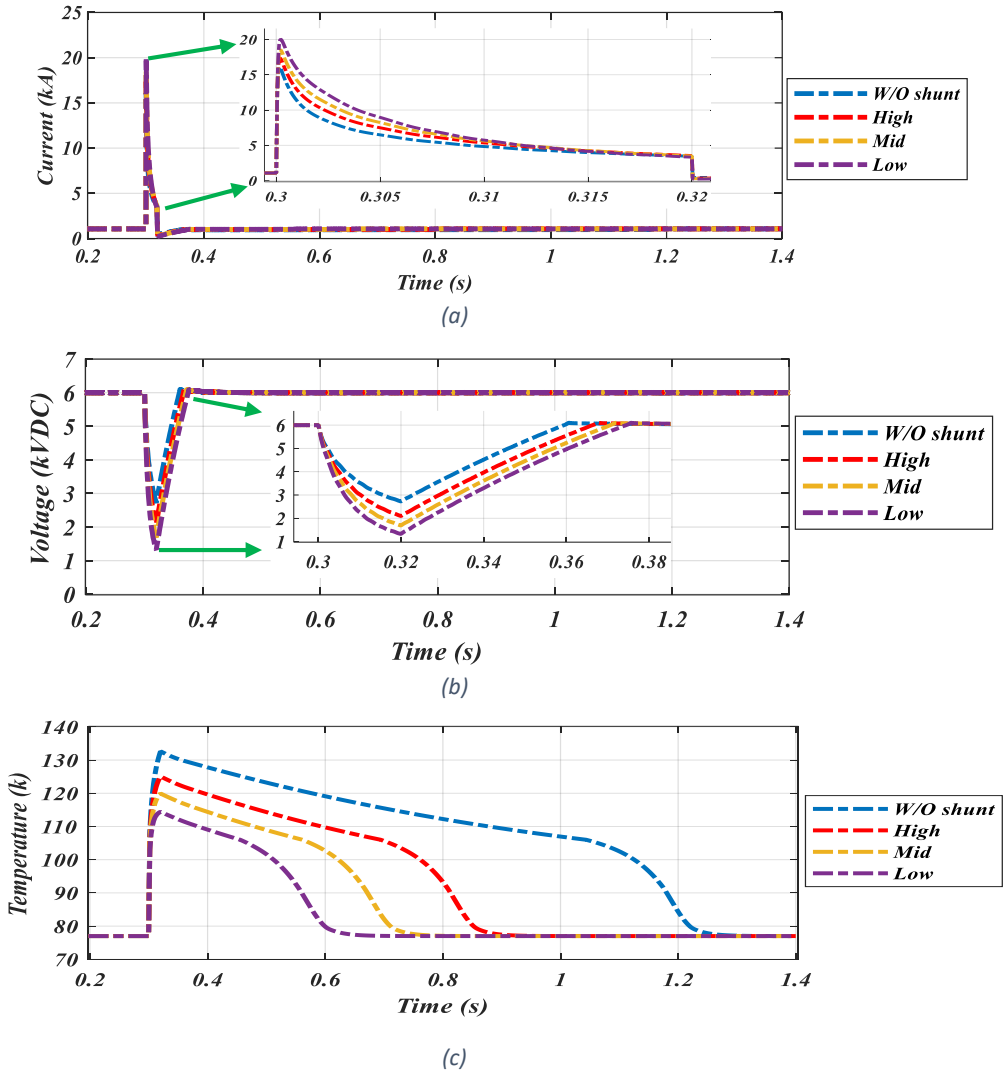


Figure 5.18: r-SFCL with 20 µm copper stabilizer with three different shunt resistors (High=2.127), (Mid= 1.0632), (Low=0.638); (a) current, (b) voltage, and (c) SFCL temperature.

Figs. 5.18 (a) and (b) demonstrate that the best current limiting capability and the less voltage drop occurred with the r-SFCL without the shunt resistor. However, as has been mentioned earlier, the shunt resistor is important for several reasons, including the safety of the r-SFCL device. The r-SFCL with the highest shunt resistor in this study shows the best performance compared with that of the mid and low resistors. The peak current with the highest resistor was 17.3 kA, while the peak current with the lowest shunt resistor was 20 kA. In contrast, the recovery time of the r-SFCL with the lowest

shunt resistor was 265 msec, while it was almost double for that with the highest shunt resistor, at 513 msec.

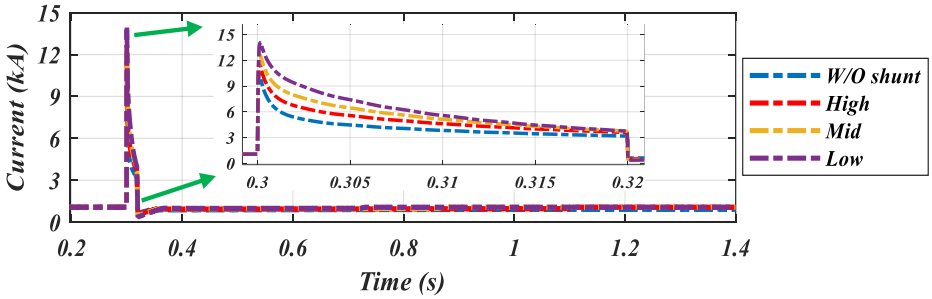
Table 5.4 compares the r-SFCL with the 20 µm copper stabilizer without and with the three different shunt resistors, namely high=2.217 Ω, mid=1.0632 Ω and low=0.638 Ω, in terms of the first peak current (kA), the highest temperature (K) and the recovery time (msec).

Table 5.4: Comparison between the first peak, the highest temp. and the recovery time of the SFCL 20 µm copper stabilizer with different shunt resistors.

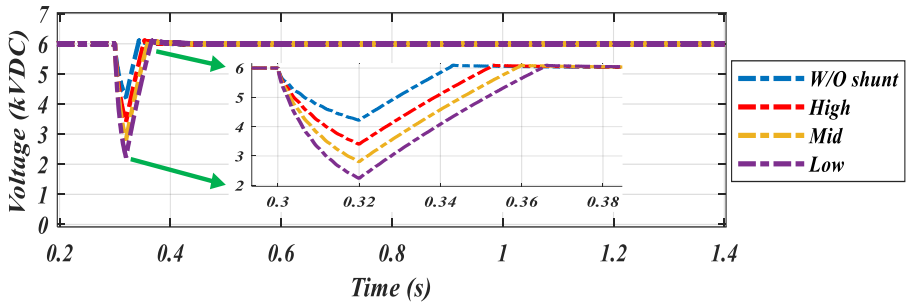
Shunt Resistor (Ω)	First Peak (kA)	Highest Temp. (K)	Recovery Time (msec)
W/O shunt	16	133	855
High=2.127	17.3	125	513
Mid=1.0632	18.5	120	372
Low=0.638	20	114.5	264

5.3.1.1.2 Case study #2 r-SFCL with 10 µm copper stabilizer

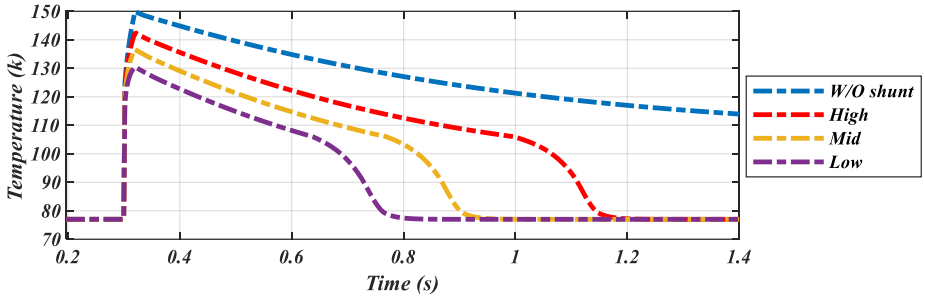
By applying the same method in the previous section, the r-SFCL with 10 µm with three different shunt resistors, calculated by Eq. 5.24, are compared in Fig. 5.19 (a), (b) and (c). The highest resistor is 200% from Eq. 5.24, which is calculated as 3.084 Ω, the medium resistor is calculated by Eq. 5.24 as 1.542 Ω, and the lowest resistor in this study is 0.925 Ω, which is the 60% of the medium resistor.



(a)



(b)



(c)

Figure 5.19: SFCL with 10 µm without and with three different shunt resistors (High=3.084), (Mid= 1.542), (Low=0.925); (a) current, (b) voltage and (c) SFCL temperature.

The r-SFCL with 10 µm without shunt resistor could not recover. However, when the shunt resistor was added to the system, the r-SFCL recovered. The recovery time of the r-SFCL with the shunt resistor is faster when the resistor is smaller. However, the peak current and the highest temperature are the highest when the resistor is the smallest.

Table 5.5 compares the r-SFCL with the 10 µm copper stabilizer without and with the three different shunt resistors, namely high=3.084 Ω, mid=1.542 Ω and low=0.925 Ω, in terms of the first peak current (kA), the highest temperature (K) and the recovery time (msec).

Table 5.5: Comparison between the first peak, the highest temp. and the recovery time of the SFCL 10 µm copper stabilizer with different shunt resistors.

SHUNT RESISTOR (Ω)	FIRST PEAK (KA)	HIGHEST TEMP. (K)	RECOVERY TIME (MSEC)
W/O shunt	10	149	Not recovered
High=3.084	11.6	142.5	810
Mid=1.542	12.66	136.5	570
Low=0.925	14.05	130.5	430

The trade-off for the r-SFCL with the shunt resistors in this study is that when the current fault limiting capability is the best, the temperature is the highest and the recovery time is the longest. For the protection study in the next chapter, the r-SFCL with the 10 µm copper stabilizer and with 3.084 Ω is chosen to characterise the r-SFCL in the transmission line in the TeA. The r-SFCL with the 10 µm copper stabilizer with the shunt resistor of 3.084 Ω has a good fault current limiting capability of up to 23.2% of the prospective current, whereby the highest temperature is in the acceptable range of the r-SFCL temperature with no risk of damage and the recovery time is less than a second (850 msec).

5.3.2 SFCL model in MATLAB/Simulink for feeder lines in TeA

This subsection demonstrates the importance of r-SFCLs in the feeder lines, even with the presence of the r-SFCL in the transmission line in the TeA. Then, the r-SFCLs are modelled and integrated/tested in the feeder lines of the TeA power system architecture.

5.3.2.1 The importance of the r-SFCLs in the feeder lines in TeA

The electrical distribution network of the TeA is a radial network, whereby the current flows in one direction from the generation side to the propulsion side. However, the upstream current has been detected as coming from VFDs' capacitors to feed Fault#2, as has been discussed in Chapter 4. In this subsection, before modelling r-SFCLs of the feeder lines, the system is subject to a fault at Fault#2 where the r-SFCL is only in the transmission line to demonstrate the need for the r-SFCLs in the feeder lines.

The system is subject to a fault at Fault#2 location, as shown in Fig. 5.20, whereby the r-SFCL is only in the transmission line at t=0.3 sec for 20 msec.

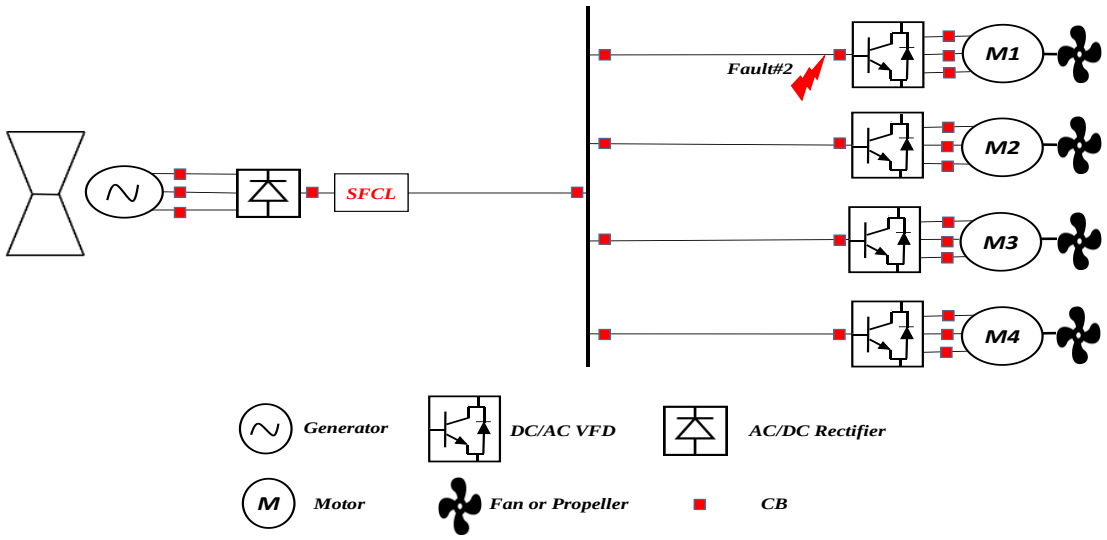
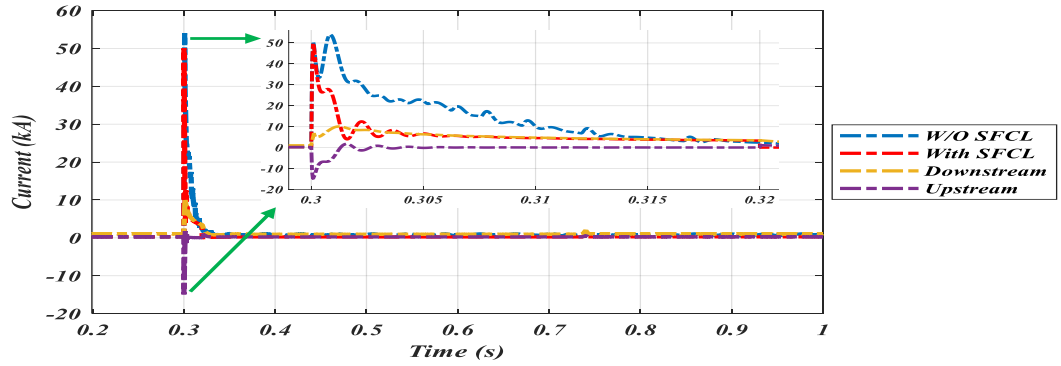
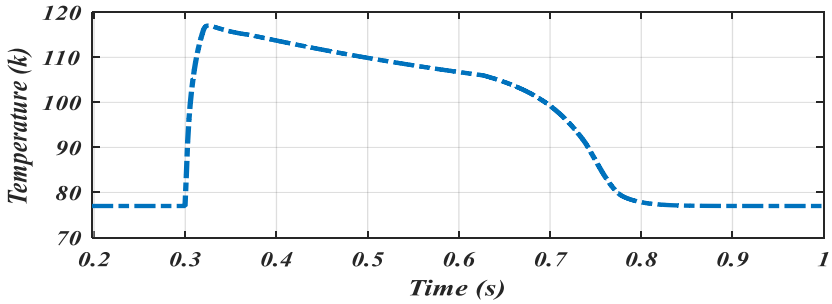


Figure 5.20: TeA power system architecture integrated with SFCL in the transmission line with Fault#2.

Fig 5.21 (a) compares the fault current at the feeder line with and without r-SFCL at the transmission line. Also, it shows the current contribution to the fault from the rectifier's and inverters' capacitors. Fig 5.21 (b) shows the temperature of the r-SFCL at the transmission line.



(a)



(b)

Figure 5.21: Fault#2 with SFCL in the transmission line only; (a) the fault current and (b) temperature of the SFCL at the transmission line.

In Fig. 5.21 (a), the blue dot-dashed line shows the current without r-SFCL at the transmission line, while the red dot-dashed line shows the fault current with the r-SFCL at the transmission line. The first peaks of the two types were almost the same because the main contribution of the first peak fault was from the inverters' capacitors upstream current. The purple dot-dashed line shows the upstream current of the capacitors of one inverter. The current was measured at the beginning of each feeder line in the downstream path (from the DC-link to the propulsion side). However, when the fault occurred, the current of the inverters' capacitors went upstream to feed the fault at location Fault#2. Hence, negative values are shown in Fig. 5.21 (a). The orange dot-dashed line shows the current coming from the rectifier side, and the r-SFCL at the transmission line was able to limit the current to less than 10 kA. Also, there was no second peak for the red dot-dashed line, as in the fault without r-SFCL, because the r-SFCL limited the current at the transmission line. The first peak of the fault with the r-

SFCL at the transmission line was mainly due to the capacitors of the inverters, which are three times the upstream current shown in this figure (3 × 15 kA) and the contribution of the capacitors of the rectifier, as shown by the orange line (5 kA for the first peak). Fig. 5.21 (b) shows the temperature of the r-SFCL at the transmission line. In order to limit the fault current of the inverter capacitors, in the next subsection, r-SFCLs are modelled and integrated into the feeder lines.

5.3.2.2 Model/Test for the SFCL in the feeder lines in TeA

For modelling the r-SFCLs for feeder lines, the r-SFCLs are designed by the same method as for the r-SFCL for the transmission line. The r-SFCL parameters are shown in Table 5.6.

Table 5.6: The design parameters of SFCLs for the feeder lines.

Parameter	Value
Critical current (A, single tape)	300
Width (mm)	12
Total thickness (μm)	70
Copper stabilizer thickness(μm)	10
Hastelloy stabilizer thickness(μm)	50
YBCO layer thickness (μm)	1
Silver layer thickness (μm)	3.8
Length of tape (m)	110
Rated voltage (kV)	6
Resistance (Ω) @100 K per tape	2.391
Resistance (Ω) @300 K per tape	7.59
Number of wires in parallel	3
Total resistance (Ω) @100 K	0.797
Total resistance (Ω) @300 K	2.53

The shunt resistor is calculated to be 200% the value of that in Eq. 5.24, namely 3.327 Ω. The fault current with the r-SFCL in the transmission line only and the fault current with the r-SFCLs in both the transmission and feeder lines are compared in Fig. 5.22 (a). The temperature of the r-SFCL in the feeder line and the temperature of the r-SFCL in the transmission line (with only one r-SFCL in transmission line) are shown in Fig. 5.22 (b).

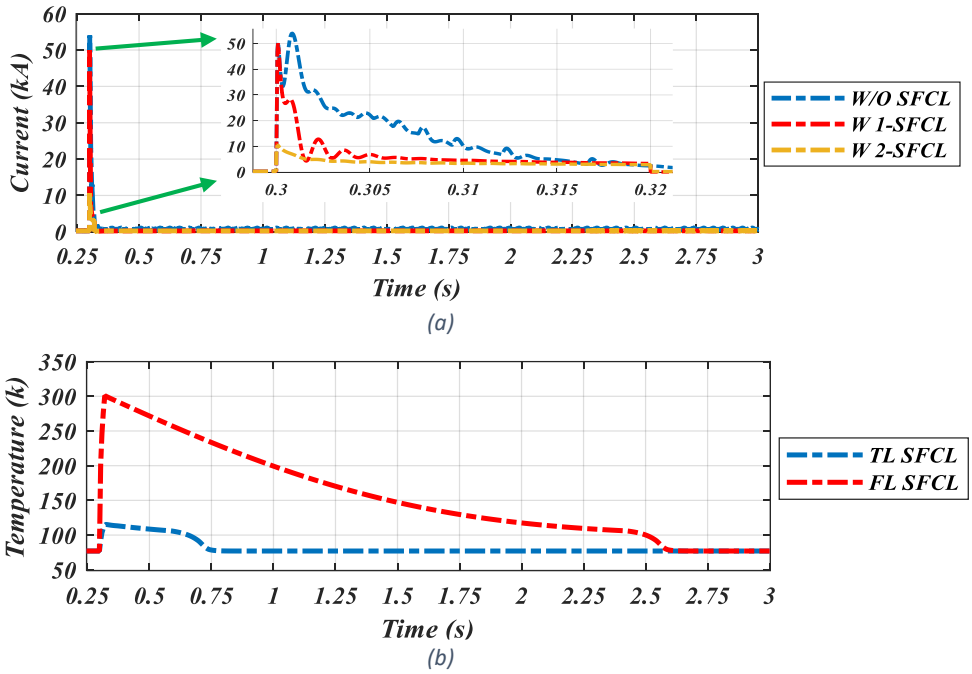


Figure 5.22: (a) Comparing the faults at Fault#2 without SFCL, with SFCL at the transmission line and with SFCLs in the transmission and feeder lines; (b) temperature of the SFCL at the transmission line and the feeders.

Fig. 5.22 (a) compares the fault current at location Fault#2, as shown in Fig. 5.22 without r-SFCLs (blue dot-dashed line), with r-SFCL at the transmission line (red dot-dashed line) and with r-SFCLs at the transmission line and the feeder lines (orange dot-dashed line). It is noticeable that after adding the r-SFCL at the transmission line, the second peak of the fault was limited, while the first peak still existed because it came from the inverters' capacitors. After adding the r-SFCL devices to the feeder lines, the r-SFCLs were able to limit the fault current to almost 10 kA, as shown by the orange dot-dashed line. Fig. 5.22 (b) shows the temperature of the r-SFCL at the transmission

line and the temperature of the r-SFCL at the feeder lines. The temperature of the r-SFCL at the feeder line is higher than the temperature of the r-SFCL at the feeder lines for several reasons: the higher current that reached the r-SFCL at the feeder line, the exposed area of the r-SFLC of the feeder line to LN_2 is much smaller than the exposed area of the r-SFCLs at the transmission line.

5.4 Chapter discussion and conclusions

Based on the TeA fault analysis in Chapter 4, two design challenges have been identified, which are the extremely high current during pole-to-pole and pole-to-ground low grounding impedance faults and the detection of the fault with the pole-to-ground high grounding impedance. In this chapter, r-SFCLs were modelled and integrated to limit the pole-to-pole fault current, which is considered the worst fault scenario in TeA power system.

The r-SFCL was designed based on the multilayer thermoelectric method, whereby each layer of the superconductor tape is calculated independently based on the temperature and the current of the r-SFCL. The current can pass through the lower resistance paths (layers), which are controlled by the current and temperature of the r-SFCL.

The impact of different copper stabilizers was demonstrated in this chapter; the results showed a trade-off between the size of the copper stabilizer, the fault current limiting capability, the temperature and the recovery time of the r-SFCL. When the copper stabilizer layer was decreased, the fault current limiting capability, the temperature of the r-SFCL and the recovery time increased, and vice versa.

Also, different shunt resistors were added to the r-SFCL devices. The shunt resistors have a great impact on r-SFCL devices. When the shunt resistor was decreased, the fault current limiting capability, temperature and recovery time were decreased, and vice versa.

Adding the r-SFCL to the transmission line limited the fault current which was coming from the rectifier's capacitors. However, when the fault occurred in the feeder line, the fault was still high because of the upstream current coming from the inverters' capacitors. After adding r-SFCLs to the feeder lines, the current was successfully limited to allow the CBs to operate safely. Fault detection, integrating CBs and power protection scenarios are discussed in the next chapter.

Chapter Six

6. The Impact of Resistive SFCLs on the Turboelectric Aircraft Power System Protection

6.1 Introduction

In Chapter 5, r-SFCLs were modelled/tested with different copper stabilizers and shunt resistors with temporary faults for a period of 20 msec. In this chapter, the r-SFCLs are integrated into the TeA power protection system to showcase the impact of the devices on system performance. One of the primary roles of the r-SFCL in the power protection system is reducing the fault current in the time gap between the fault occurrence and the fault clearance. When a fault occurs, the fault detection system detects the fault and then sends signals to the CBs to operate/clear the fault. The operational time of the detection system and CBs determines the time gap between the fault occurrence and the fault clearance. The r-SFCLs are in charge of reducing the fault current, maintaining a stable operation for the healthy lines in the system, and ensuring safe CBs operation.

This chapter starts by describing the fault detection methods in DC power systems, including the overcurrent detection method, current differential detection method, and undervoltage detection method. A review of DC circuit breakers is presented in this chapter for different time clearances. Fault scenarios at the feeder line are performed to show the impact of the r-SFCL on the power system protection. The r-SFCLs are tested with different CB response times to show the effectiveness of the devices on reducing the fault currents and ensuring safe operation of the CBs.

6.2 Fault detection methods in DC power systems

After demonstrating the DC fault behaviours in the TeA power system in Chapter 4, several points have to be considered to choose an effective fault detection method in the TeA DC power system: a) the extremely high fault magnitude in pole-to-pole and pole-to-ground low grounding impedance faults; b) the fast change rate of the fault in the DC system; and c) the low fault current magnitude in some cases, as in the pole-to-ground fault with high grounding impedance, where it is less than the rated current.

6.2.1 Overcurrent detection method

One of the simplest fault detection methods is the overcurrent detection (OC) method. An obvious indication of a fault occurrence is a sharp increase in the DC current. It only needs a sensor to monitor the DC current, whereby if there is a vast increase in the DC current, a signal will be sent to the CB to operate and isolate the fault [160].

The threshold value is an essential parameter for the overcurrent detection method for each CB. In TeA based on 6 kVDC, the pole-to-pole and pole-to-ground low grounding impedance faults can be safely detected by the overcurrent detection method. Fig. 6.1 shows the three different zones based on the peak fault depending on the ground impedances (for pole-to-ground fault). In zone #1, the overcurrent detection method can be safely used as the fault current is higher than the rated current in addition to a 50% safety margin to ensure no false detection. The threshold value is calculated as 3 kA in this study. With a pole-to-pole fault, the overcurrent detection method can be used safely. However, with a pole-to-ground fault, the grounding impedance has to be less than 1.07 Ω to be detectable by the overcurrent detection method.

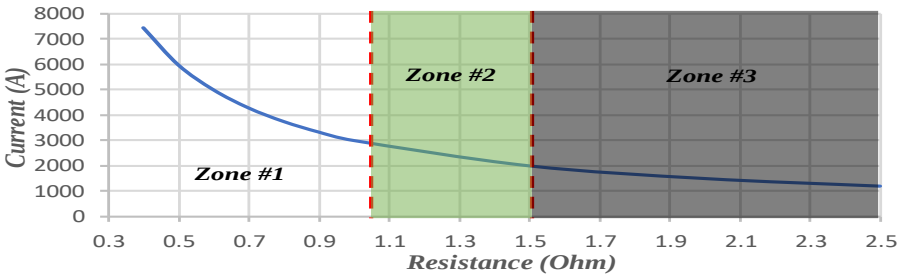


Figure 6.1: Fault detection method determination based on the fault current magnitude zones for the transmission line in TeA..

To investigate the OC detection method for the TeA power system, firstly, white Gaussian noise is added to the original signal of 30 dB. Secondly, faults are applied to the system at Fault#1 with four different cases, namely pole-to-pole (PP) fault with r-SFCL, pole-to-ground (PG) with 0.5 Ω grounding impedance (zone #1), PG with 1.2 Ω grounding impedance (zone #2), and PG with 2.1 Ω grounding impedance (zone #3).

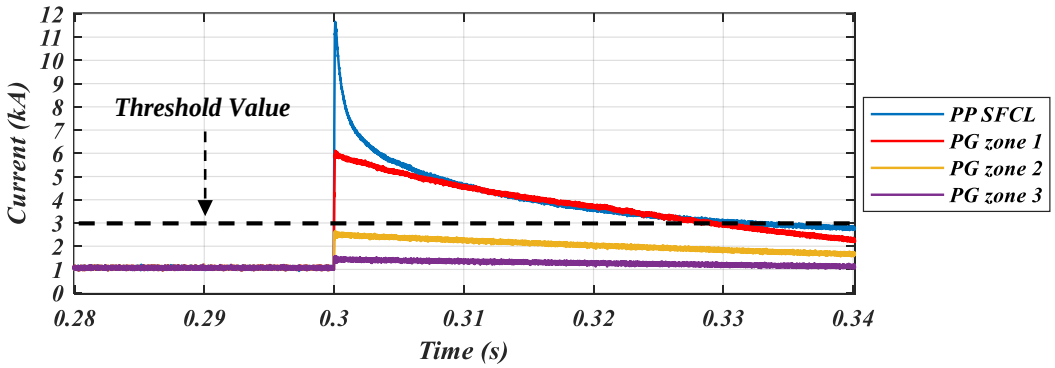


Figure 6.2: OC detection method with four different fault cases.

With the OC detection method, the fault currents are detected for PP with r-SFCL and for the pole-to-ground fault in zone 1 (PG zone 1, up to 1.07 Ω grounding impedance). However, when the grounding impedance is higher than 1.07 Ω, the fault current is still under the threshold value; therefore, it is not detectable by the OC detection method.

6.2.2 Current differential detection method

Unlike the OC detection method, which is considered a non-unit protection method, the current differentional (CD) detection method is a unit protection method. The protection

unit in the TeA power system can be used for a DC line, a busbar or a converter station. Fig. 6.3 shows the CD detection method in the transmission line. Under normal operation, I_1+I_2 should equal approximately zero (or up to 25% of the rated current, depending on the protection setting), where I_1 is the current passing through CT1 and I_2 is the current passing through CT2. If the total of I_1+I_2 is higher than the threshold value, there is a fault in the protected unit. Thus, signals are sent to the CBs to isolate the faulted line/equipment.

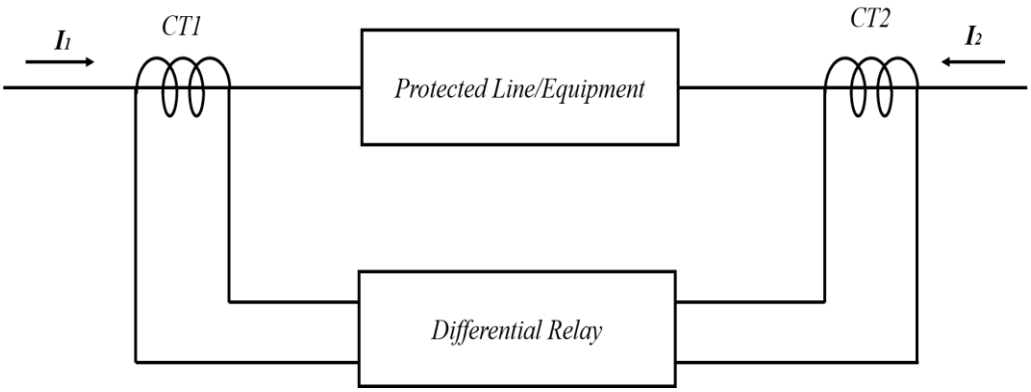


Figure 6.3: Current differential detection method concept.

The TeA power system architecture is subjected to five different faults at the Fault #1 location. The threshold value is set to 25% of the rated current during take-off. Fig. 6.4 shows the fault with the five different cases in the CD detection method.

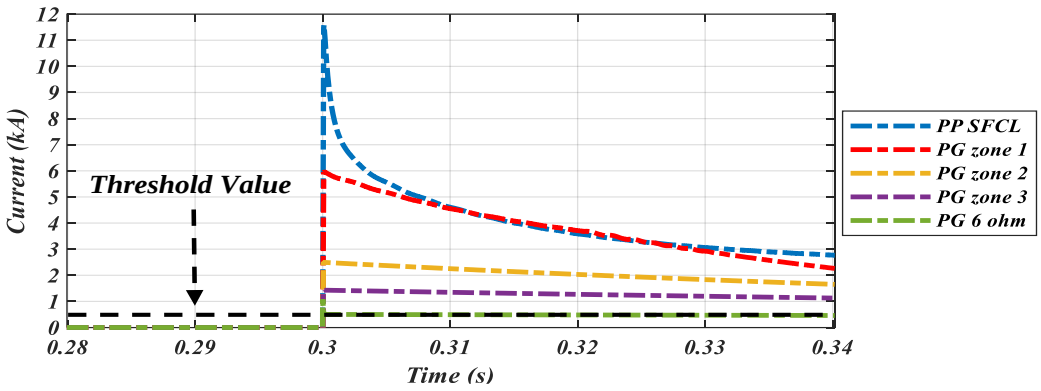


Figure 6.4: CD detection method with five different fault cases.

With the CD detection method, the fault currents are detectable with up to 6 Ω grounding impedance with a threshold value setting of up to 25 % of the rated current. The CD detection method can detect the fault with higher grounding impedance compared to the OC detection method. Also, the CD detection method has a high selectivity capability compared to the OC detection method [161].

6.2.3 Undervoltage detection method

A voltage drop of the DC link which is caused by the fault in the system can be measured and compared to a pre-defined value to be used as a threshold value to operate CBs. The threshold value can be determined based on the IEEE standard for MVDC power systems 1709-2018 [137]. According to the IEEE standard 1709-2018, MVDC voltage tolerance limits should be ± 10%. In this study, the threshold values are set to 0.9 and 1.1 pu of the DC-link voltage (5.4 and 6.6 kV). Fig. 6.5 shows the voltage drops between the positive and negative poles during faults for two cases.

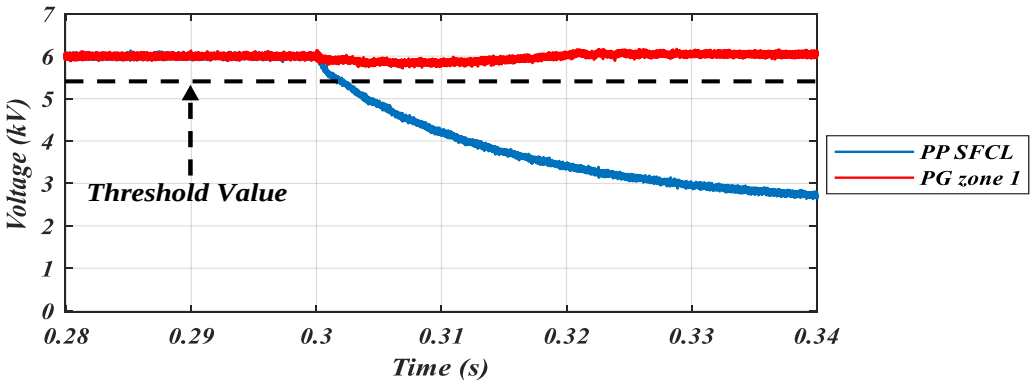
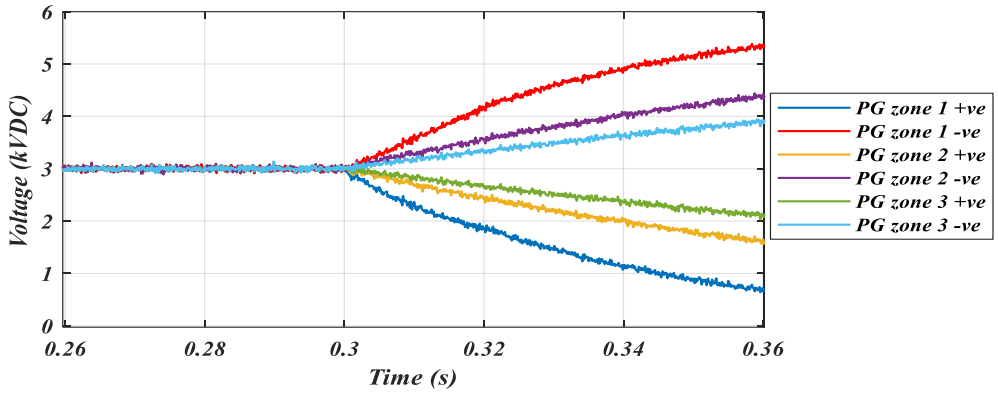


Figure 6.5: Under-voltage detection in the DC link voltage by measuring the difference between the positive and negative poles.

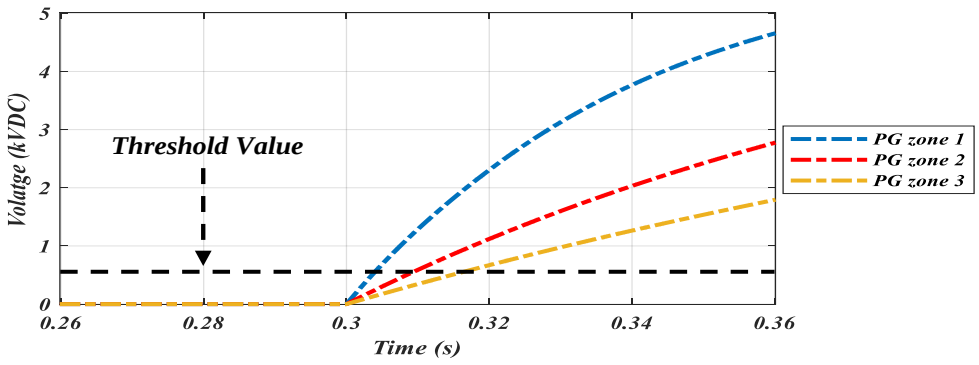
The blue line indicates the voltage of the DC-link when a pole-to-pole fault occurs at Fault#1 with the presence of the r-SFCL. The voltage hits the threshold value after 1.92 msec. The r-SFCL slows down the discharge time of the capacitor. However, it only

takes 7.86 µsec for the current to hit the threshold value with the overcurrent detection method. The UV detection method can be used as a backup detection method for pole-to-pole faults. The red line indicates the voltage of the DC link when a pole-to-ground fault with grounding impedance 0.5 Ω (zone 1) occurs. By measuring the voltage potential between the +ve and -ve poles, the UV detection method cannot detect the fault because the healthy pole compensates the faulty pole, as has been explained in Chapter 4.

For pole-to-ground faults, it is possible to use the UV detection method to detect the fault, but by measuring the difference between the voltages of the positive and negative poles. In this study, the voltage of the positive pole is 3 kVDC (ground to positive pole), and the voltage of the negative pole is 3 kVDC (ground to negative pole). Fig 6.6 (a) and (b) show the poles' voltage and the difference between them, respectively.



(a)



(b)

Figure 6.6: Pole-to-ground fault for different zones.

Fig. 6.6 (b) shows the voltage differences between the +ve and -ve poles for zone 1 (0.5 Ω), zone 2 (1.2 Ω) and zone 3 (2.1 Ω) pole-to ground faults with the blue, red and orange lines, respectively. With low ground impedance (0.5 Ω), the threshold value is hit after 4.4 msec. However, with zone 3 (2.1 Ω), the threshold value is hit after 18 msec. By subtracting the poles' voltages, it is possible to detect the pole-to-ground faults. Although this method is still relatively slow, it can be used as a backup protection method.

6.2.4 Voltage and current derivative (dv/dt) and (di/dt) detection methods

Both the voltage derivative (dv/dt) method and current derivative (di/dt) method work on the same working principle by predefining threshold values. The threshold values are compared to the rates of change of the current/voltage in the system. If the rates of change of the current/voltage are higher than the pre-defined values, a signal will be sent to the CBs to operate. This method offer the advantage of quick detection. However, the derivative methods suffer from limited selectivity due to low line impedance, especially in compact networks like those in TeA [162]. Moreover, this method is sensitive to noise due to the use of derivation, which can result in false detection signals [163].

6.3 The impact of r-SFCLs on protection system response time

The previous two subsections described fault detection methods and DC circuit breakers. The fault isolation time is determined by the fault detection time and the operational speed of the DC circuit breaker. The operational speed of the DC circuit

breaker is the dominant factor in the fault isolation time [67]. There have been several lab-scale hybrid DC circuit breakers, which take 4 to 5 ms to isolate the fault [69], [73].

In this section, a pole-to-pole fault is applied to the system at t=0.3 sec at the Fault#2 location, as shown in Fig. 6.11. The clearance time of the fault was chosen to be 4 msec to up to 64 ms to demonstrate how the r-SFCL works in mitigating the impact of the fault between the fault occurrence and the fault clearance. The 4 msec was chosen based on the fastest operational time of reported hybrid DC CBs in the literature review.

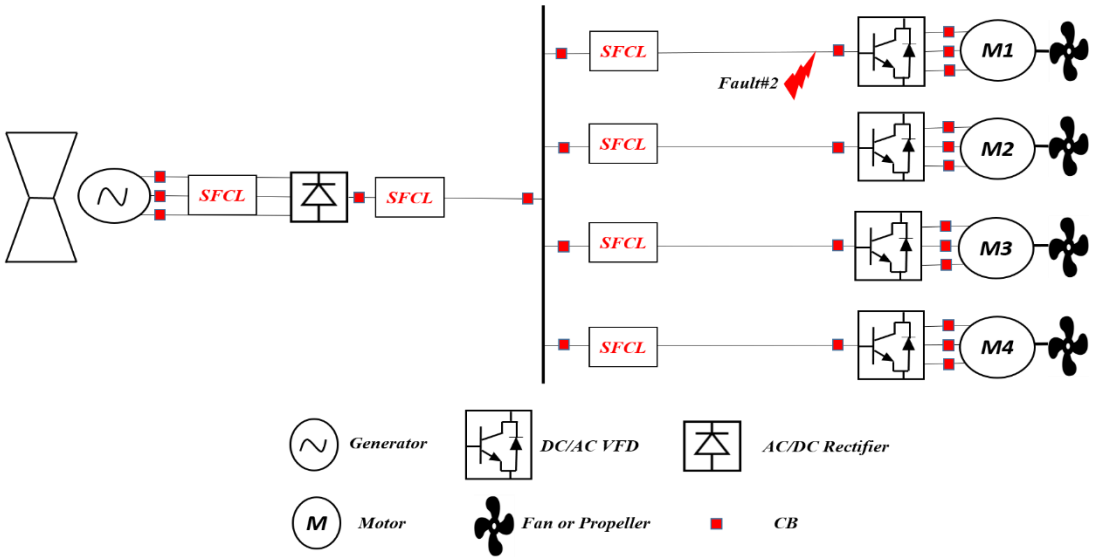


Figure 6.7: The TeA power system architecture, including the r-SFCLs and Fault#2 location.

Fig. 6.12 (a) shows the current at the feeder line of the M1 motor. Fig. 6.12 (b) shows the DC bus voltage during the fault whereby the CB was able to isolate the faulty feeder in 4 msec with and without the r-SFCL. The 4 msec was chosen based on the time response in the previous two subsections. Fig. 6. 12 (c) shows the motors' speed in healthy branches, specifically M4. Fig. 6. 12 (d) shows the temperature of the faulty feeder's r-SFCL.

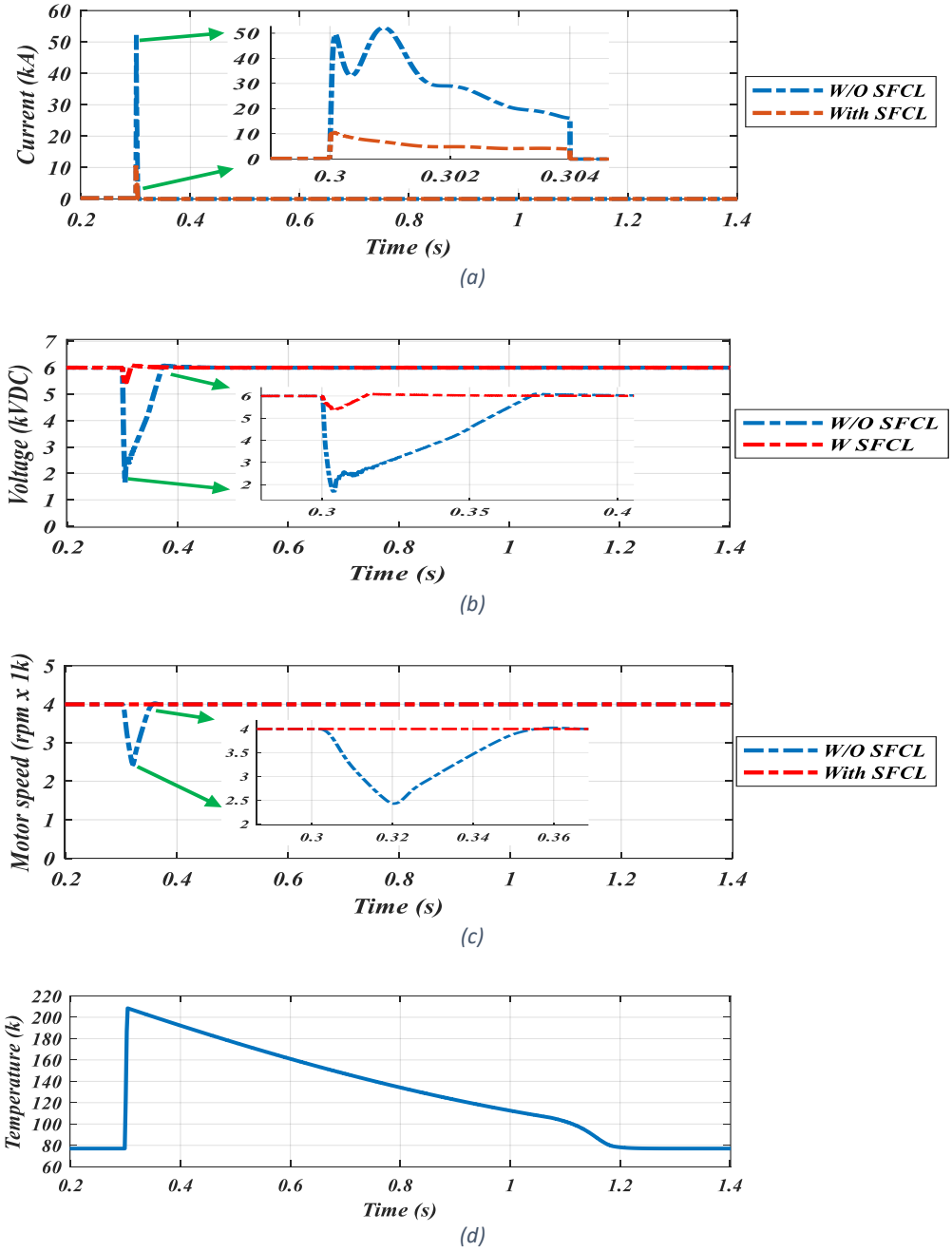
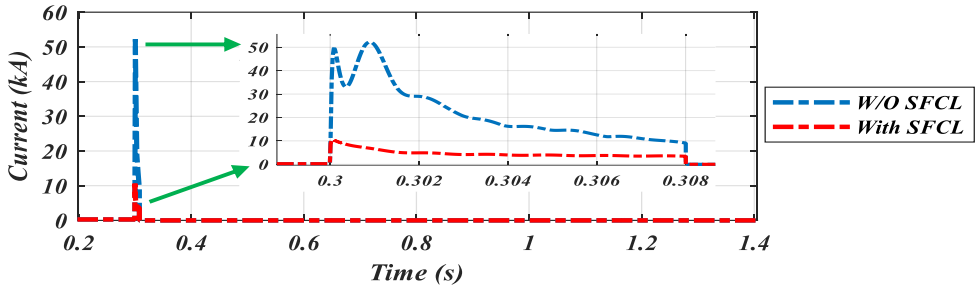


Figure 6.8: Impact of the r-SFCL on the power protection system with 4 msec clearance time; (a) current, (b) voltage, (c) motor speed (M4) and (d) r-SFCL temperature.

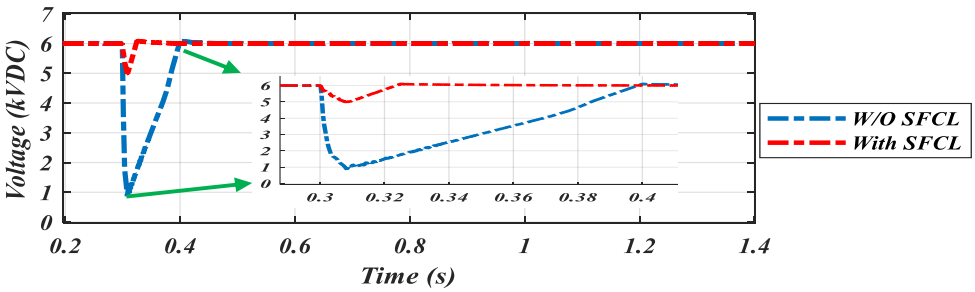
In this scenario, the CB was able to isolate the faulty feeder in 4 msec. Fig. 6. 12 (a) shows that the first peak of the fault current was almost 10 kA with the r-SFCL, while it reached to 50 kA without the r-SFCL. Reducing the fault current in the faulty feeder helped in reducing the voltage drop in the DC bus voltage, as shown in Fig. 6.12 (b). Without the r-SFCL, the voltage dropped to almost 2 kVDC and took approximately 60 msec to recover, while with the r-SFCL, the voltage dropped to 5.5 kVDC and

recovered in less than 20 msec. Because the voltage drop at the DC bus with the r-SFCL was just less than 8.3 % of the rated voltage and lasted less than 20 msec, the motor speed (healthy feeders, specifically M4) was stable even with the fault occurrence in the faulty feeder, as shown in Fig. 6. 12 (c). Fig. 6. 12 (d) shows the temperature of the r-SFCL in the faulty feeder, reaching 210 K, which is considered a safe temperature for the r-SFCL coils.

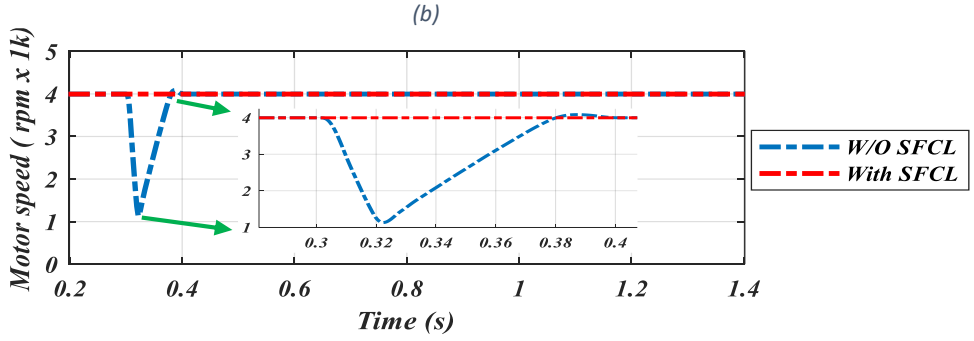
Fig. 6. 13 (a), (b), (c) and (d) show the current at the faulty feeder, the voltage at the DC bus, and the motor speed (M4) and the r-SFCL of the faulty feeder, respectively. The clearance time in this scenario is 8 msec.



(a)



(b)



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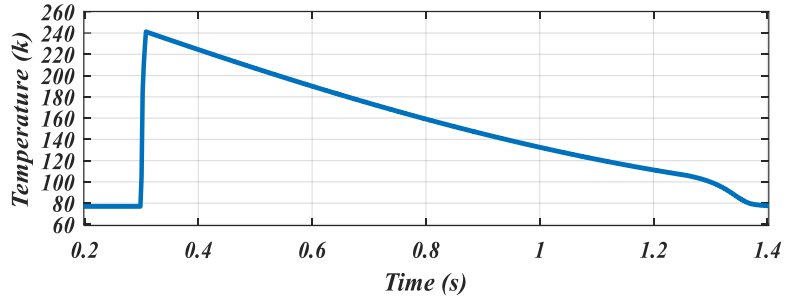
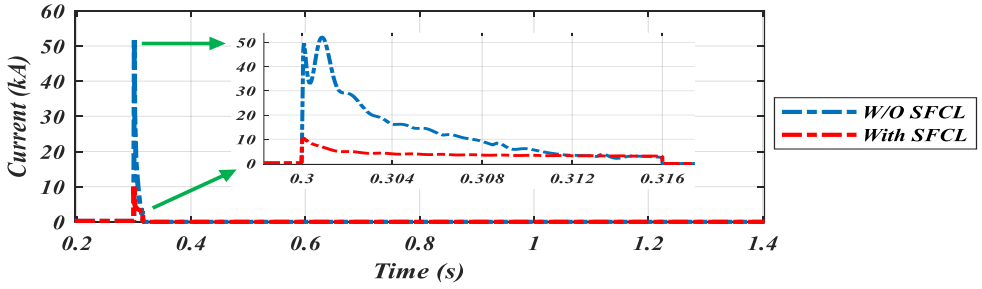


(d)

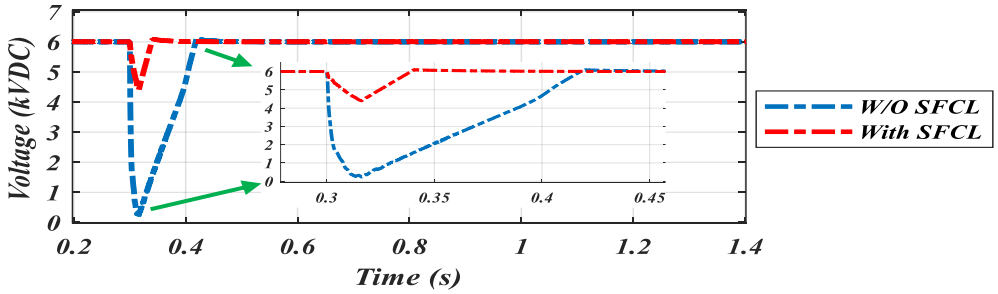
Figure 6.9: : Impact of the r-SFCL on the protection system with 8 ms clearance time; (a) current, (b) voltage, (c) motor speed (M4) and (d) r-SFCL temperature.

When the time gap between the fault occurrence and fault clearance increased to 8 msec, the voltage at the DC bus dropped to 5 kVDC with the r-SFCL compared to 5.5 kVDC with the 4 msec clearance time, as shown in Fig. 6. 13 (b). The r-SFCL's temperature for the faulty feeder increased to 240 K compared with the 210 K with the 4 msec fault clearance, as shown in Fig. 6. 13 (d). The motors' speeds in healthy feeders were still stable even with the 8 msec fault clearance, as shown in Fig. 6. 13 (c).

Fig. 6. 14 (a), (b), (c) and (d) show the current at the faulty feeder, the voltage at the DC bus, the motor speed of M4 (healthy feeder) and the temperature of the r-SFCL of the faulty feeder, respectively. The clearance time in this scenario is 16 msec.



(a)



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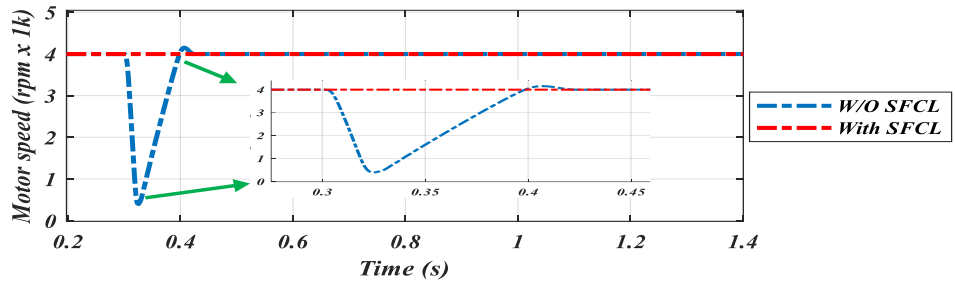

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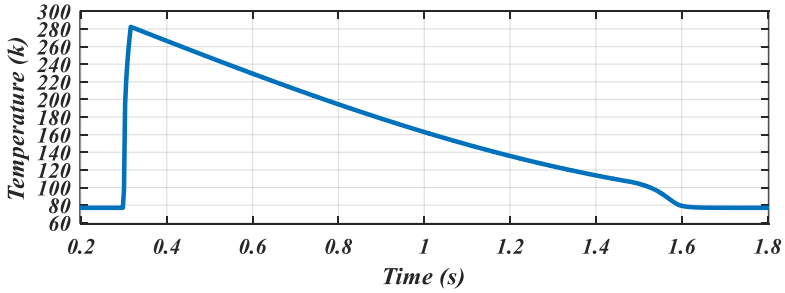
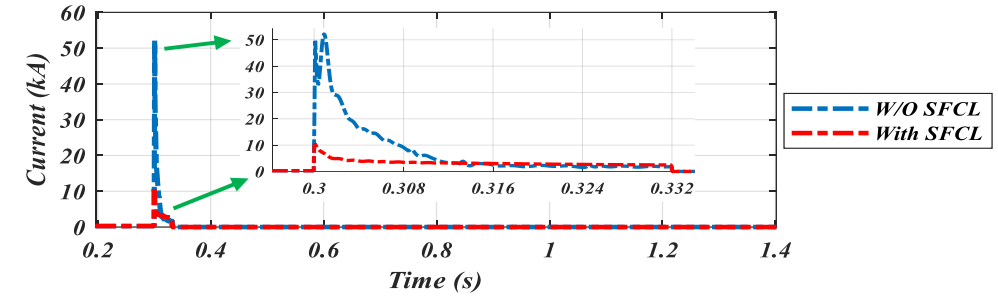


(d)

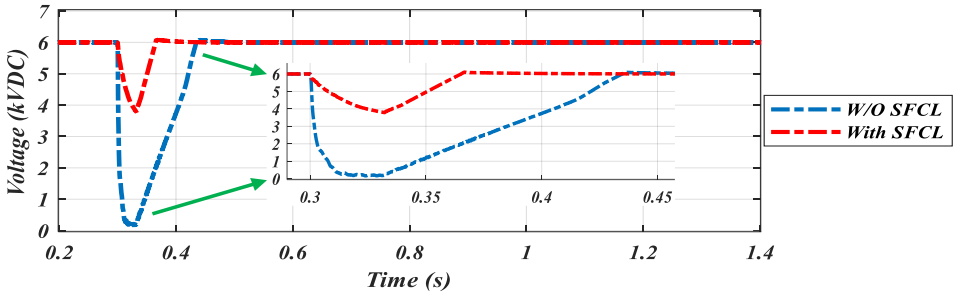
Figure 6.10: Impact of the r-SFCL on the protection system with 16 ms clearance time; (a) current, (b) voltage, (c) motor speed (M4) and (d) r-SFCL temperature.

When the time gap between the fault occurrence and fault clearance increased to 16 msec, the voltage at the DC bus dropped to 4.4 kVDC with the r-SFCL, while it dropped to almost zero without the r-SFCL, as shown in Fig. 6. 14 (b). The r-SFCL's temperature for the faulty feeder increased to 280 K compared with the 240 K with the 8 msec fault clearance, as shown in Fig. 6. 14 (d). The motors' speeds in healthy feeders are still stable even with the 16 msec fault clearance, as shown in Fig. 6. 14 (c).

Fig 6.15 and Fig 6.16 present the system performance during the faults at the Fault#2 location with and without the r-SFCL with time clearances of 32 msec and 64 msec, respectively.



(a)



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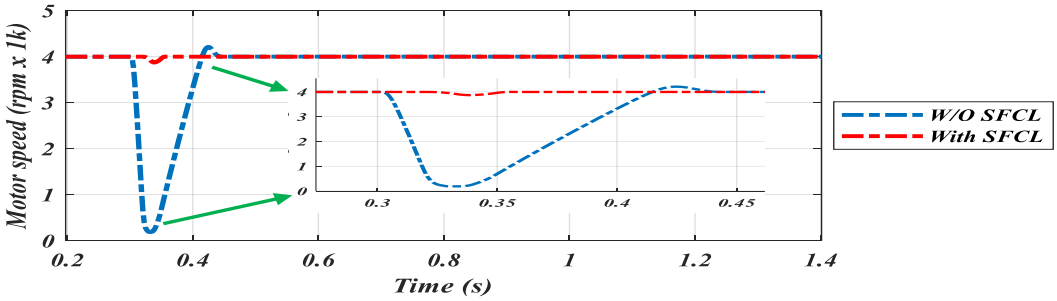

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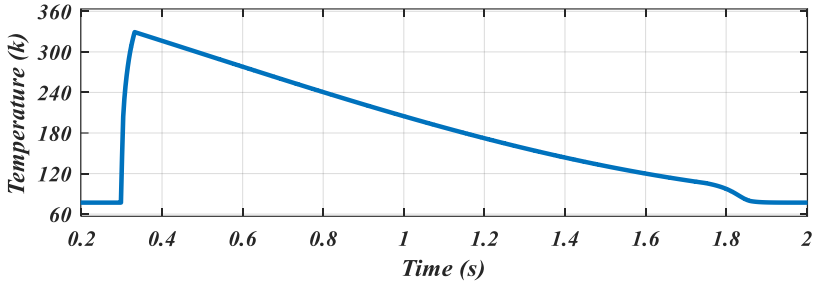

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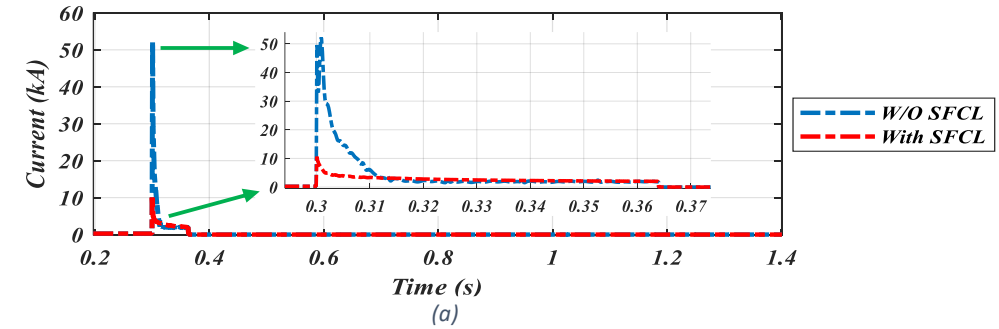
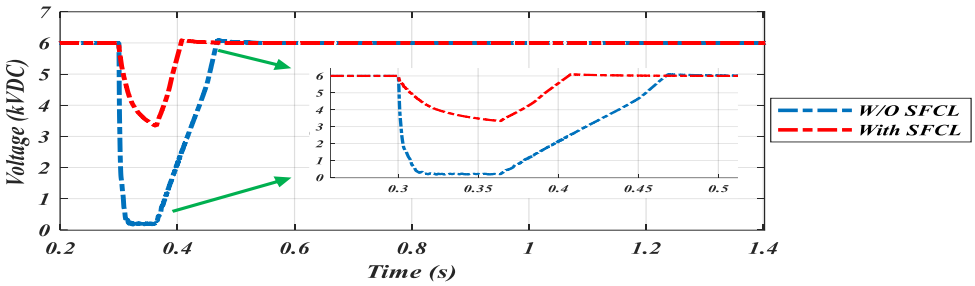
Figure 6.11: Impact of the r-SFCL on the protection system with 32 msec clearance time; (a) current, (b) voltage, (c) motor speed (M4) and (d) r-SFCL temperature.



(a)



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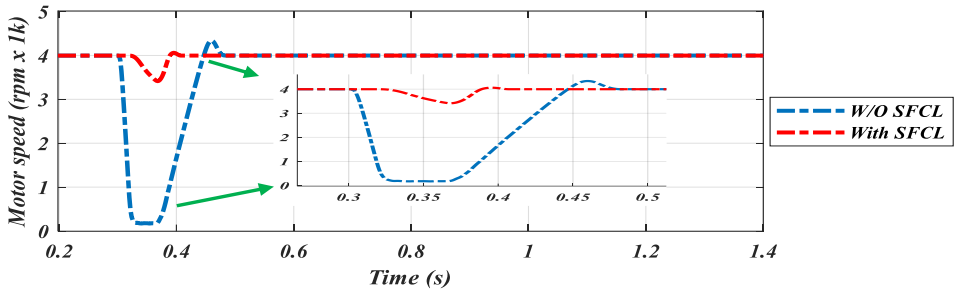

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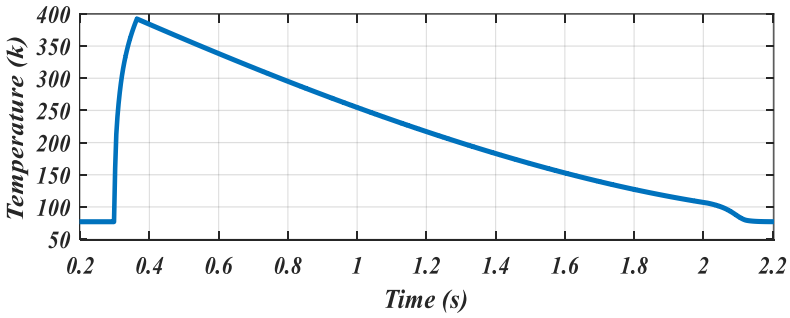


(d)

Figure 6.12: Impact of the r-SFCL on the protection system with 64 msec clearance time; (a) current, (b) voltage, (c) motor speed (M4) and (d) r-SFCL temperature.

It is noticeable that when the time gap between the fault occurrence and the fault clearance increases, the fault impact on the system performance increases. However, the integrated r-SFCLs of the TeA power system were able to mitigate the impact of the fault, reduce the voltage drop in the DC bus, and maintain the propulsion system at the required speed.

Fig. 6.17 shows the performance of the system with the five different time clearances. The motors' speeds in the healthy feeder were stable up to a 16 msec time gap. When the time gap went up to 32 msec, the motors' speeds dropped to just above 3800 rpm.

With 64 msec time clearance, the motors' speeds dropped to 3600 rpm, as shown in Fig. 6. 17 (c). Fig. 6. 17 (d) shows the temperatures of the r-SFCLs in the faulty branch. With the 4 msec time clearance, the temperature of the r-SFCL was 210 K, while the highest temperature occurred with the longest time gap, 64 msec, reaching 390 K.

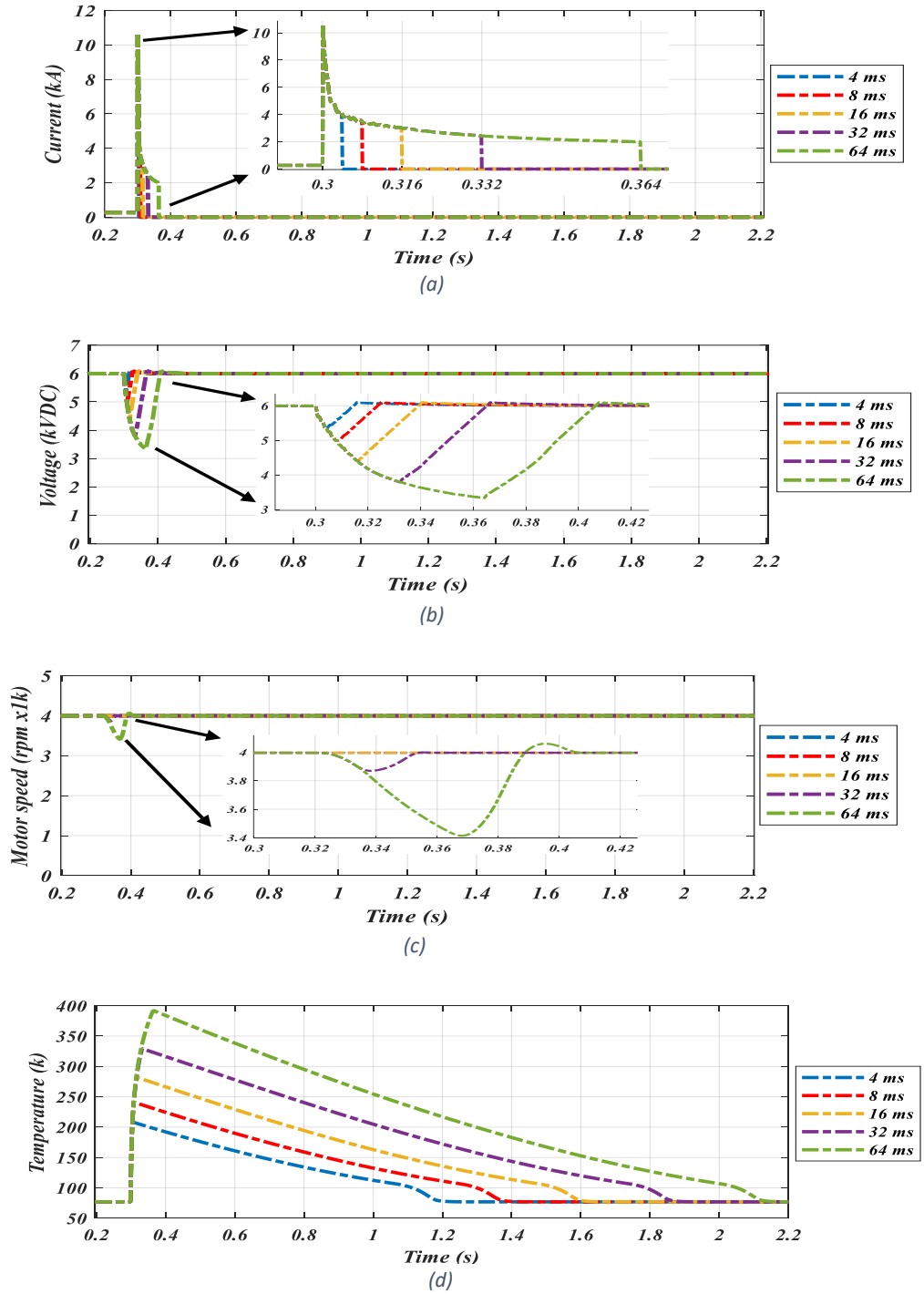


Figure 6.13: Comparisons between the five fault scenarios with the r-SFCLs for 4, 8, 16, 32, and 64 msec time gaps between the fault occurrence and fault clearance.

6.4 Chapter discussion and conclusion

This chapter started by demonstrating the causes for the time gap between the fault occurrence and the fault clearance, which is the operational time of the the fault detection system and CBs. Different fault detection methods and CBs were demonstrated, including their working principle and operational time. The impact of the r-SFCLs is demonstrated in the TeA power system by performing a fault scenario at the feeder line.

The CD detection method can detect a pole-to-ground fault with high grounding impedances up to 6 Ω, whereas the OC detection can only detect faults up to 1.07 Ω. In addition, the CD detection method is a unit protection method which ensures a high protection selectivity for the system. However, the CD detection method needs communication between the two sides of the protected device (line in this study), whereas it is not required in the OC method. Because the line length is relatively short, up to 40 m, the communication will not cause a significant delay; therefore, the CD detection method can be the main detection method and OC/UV can be used as backup detection methods.

Integrating r-SFCLs into the TeA power system supports the protection system by reducing the fault current, reducing the voltage drop at the main DC bus, and therefore improving the stability of the speed of the motors in the healthy feeders. Based on the results in this chapter, the TeA power protection system offers a better performance with the r-SFCLs with the 64 ms time gap than even the 4 ms scenario without r-SFCLs in terms of fault currents, voltage drop and motor speed stability.

The ideal case for the power protection system is to always have fast CBs to isolate faults. However, while it is not currently possible to find fast CBs with low on-state

losses, the r-SFCLs can mitigate the impact of the fault in the time gap between the fault occurrence and the fault clearance, giving CBs sufficient time to operate safely. Besides, r-SFCLs increase the flexibility of the power protection system design to ensure a high level of protection system selectivity and granularity.

Chapter Seven

7. Superconducting Magnetic Energy Storage for Stability Improvement in Turboelectric Aircraft

7.1 Introduction

In this chapter, the power system architecture of the TeA was finalised by integrating SMES to the SFCL. This chapter starts by describing the power generation unit constraints in TeA. The SMES's control method is illustrated in this chapter, including the three operational moods; charge mode, discharge mode and standby mode. Finally, two simulation results are shown and compared where SMES works as a backup power source to support the propulsion system during temporary power loss. The weight and size of SMES are considered for both case studies.

There are several constraints on the power generated by generators, including power equilibration limits, limits of the generator's active power, and the ramp-rate limits [164]–[166]:

$$\sum_{j=1}^{G} P_{ij} = P_{Di} + P_{Li} \;\; i = 1,2,\dots,N \tag{7.1}$$

$$P_j^{min} \leq P_{ij} \leq P_j^{max} \quad i = 1,2,..,N, j = 1,2,\dots,G \tag{7.2}$$

$$\frac{P_i(n) - P_i(n-1)}{\Delta t} \leq k \tag{7.3}$$

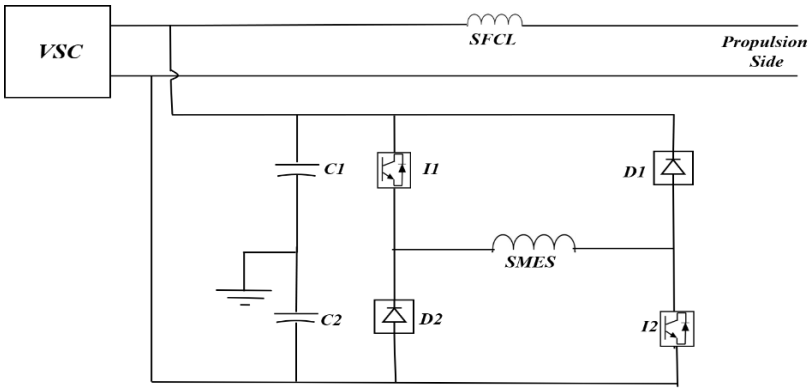
Where P_{Di} is the total system load and P_{Li} is the total system loss. P_j^{min} and P_j^{max} are the upper and lower allowable active power outputs of generator j, respectively. $P_i(n)$ and $P_i(n-1)$ are the output powers of the generator in two different moments Δt, and

k is the allowable ramp-rate of the generator. Because the TeA power system architecture is a highly dynamic system, adding SMES can reduce the stresses on the on-board power generation units. In addition, SMES can work as a backup power source for short periods of time to mitigate any unexpected intermittent electrical output effects from the generation unit in the AC side.

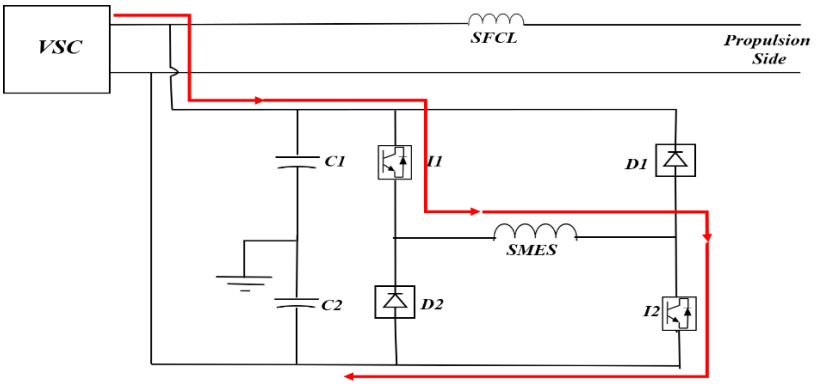
7.2 SMES control method

The main goal of adding SMES to the power system architecture is to ensure the stable operation of the propulsion system during unexpected intermittent power losses in the AC side. The main principle of the control strategy is to generate different pulses in the SMES converter to control the charging and discharging of the SMES. The SMES is controlled by logical functions, which compares the main bus voltage and the voltage reference and considers the state of charge (SOC) of the SMES by taking feedback of the stored current (*Ismes*). When the voltage and current of the main transmission line drop to below *Vref(min)* and *Iref(min)*, the SMES discharges immediately to feed the load and maintain the main bus voltage, thus maintaining the propulsion system's speed. The main idea of measuring the current in the transmission line is to differentiate between the DC fault in the DC side and the intermittent fault in the AC side. The main DC bus voltage is maintained within the required range (*Vref(min)* < *Vbus* < *Vref(max))*. According to the IEEE standard 1709-2018 [137], the DC voltage tolerance limits should be ± 10%. However, the tolerance limit was tightened to ± 3% in order to improve system stability, as this was one of the main goals of this study. Thus, *Vref(min)* is 0.97 pu of the nominal voltage, and *Vref(max)* is 1.03 pu of the nominal voltage.

The H-bridge DC/DC converter is used to control the charging and discharging of the SMES. It consists of two diodes (D1, D2) and two IGBTs (I1, I2), as shown in Fig. 7.3 (a). There are three operation modes: the charge mode, the discharge mode and the standby mode. The different modes of the SMES are controlled by *Vref(min), Vref(max), Idc(min), Idc(max), Ismes(min)* and *Ismes(max),* where these reference points are set to operate the SMES safely and effectively. The goal of this control method is to maintain the voltage of the DC bus at the rated voltage (6 kVDC), and thus maintain the propulsion system's speed at the required speed. The three operation modes are shown in Fig. 7.1.



(a)



(b)

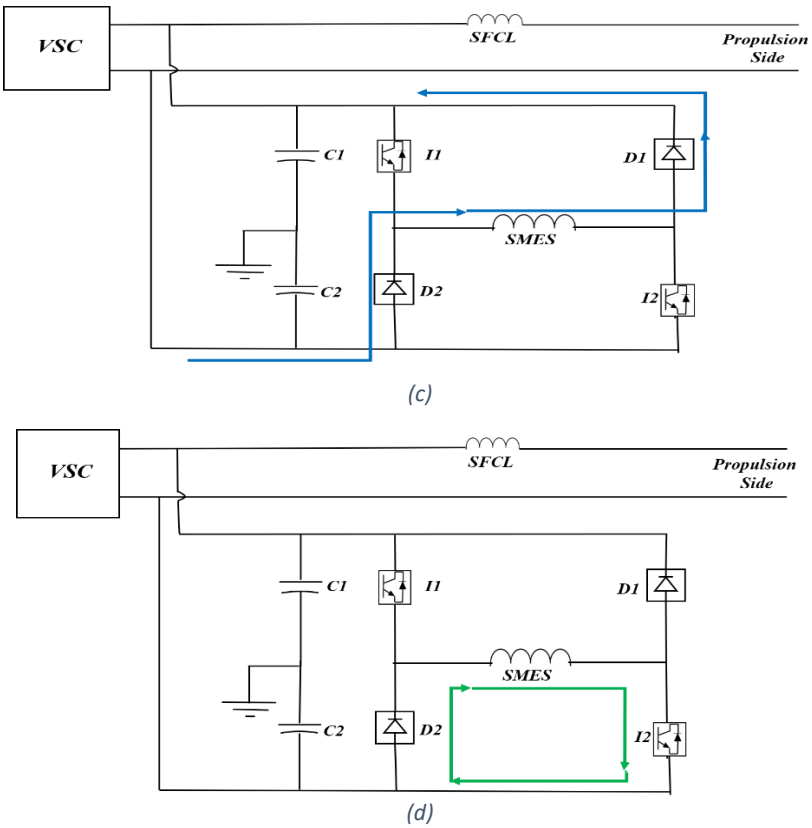


Figure 7.1: The DC/DC H-bridge converter of SMES with three operation modes; (a) circuit topology, (b) charging mode, (c) discharging mode, (d) standby mode.

7.2.1 Charge mode

In charge mode, the controller is switching between conduction paths in Fig. 7.1 (b) and (d); where d2 (the duty ratio of I2) is continuously on (i.e. 1), while d1 (the duty ratio of I1) is switching between on and off, thus allowing the SMES to store the required amount of current to maintain the DC bus voltage at the reference value for the length of time it was designed for. In order to control the charge rate of SMES and prevent overcharge of SMES, logical functions are used to control the duty ratios d1 and d2.

7.2.2 Discharge mode

In discharge mode, the controller is switching between conduction paths in Fig. 7.1 (c) and (d); where d1 (the duty ratio of I1) is continuously off (i.e. 0), while d2 (the duty ratio of I2) is switching between on and off to allow the SMES to discharge the required

amount of current to maintain the DC bus voltage at the reference value. In order to control the discharge rate of SMES and prevent over-discharge of SMES, logical functions are used to control the duty ratios d1 and d2.

7.2.3 Standby mode

In standby mode, the bus voltage is in the acceptable range between 0.97 and 1.03 pu of the nominal voltage. Hence, no output current from SMES is needed. To keep the current circulating between D2 and I2, d1 (the duty ratio of I1) is continuously off (i.e. 0) and d2 (the duty ratio of I2) is on constantly (i.e. 1). Fig. 7.2. shows a flowchart to demonstrate the conditions of each operation mode.

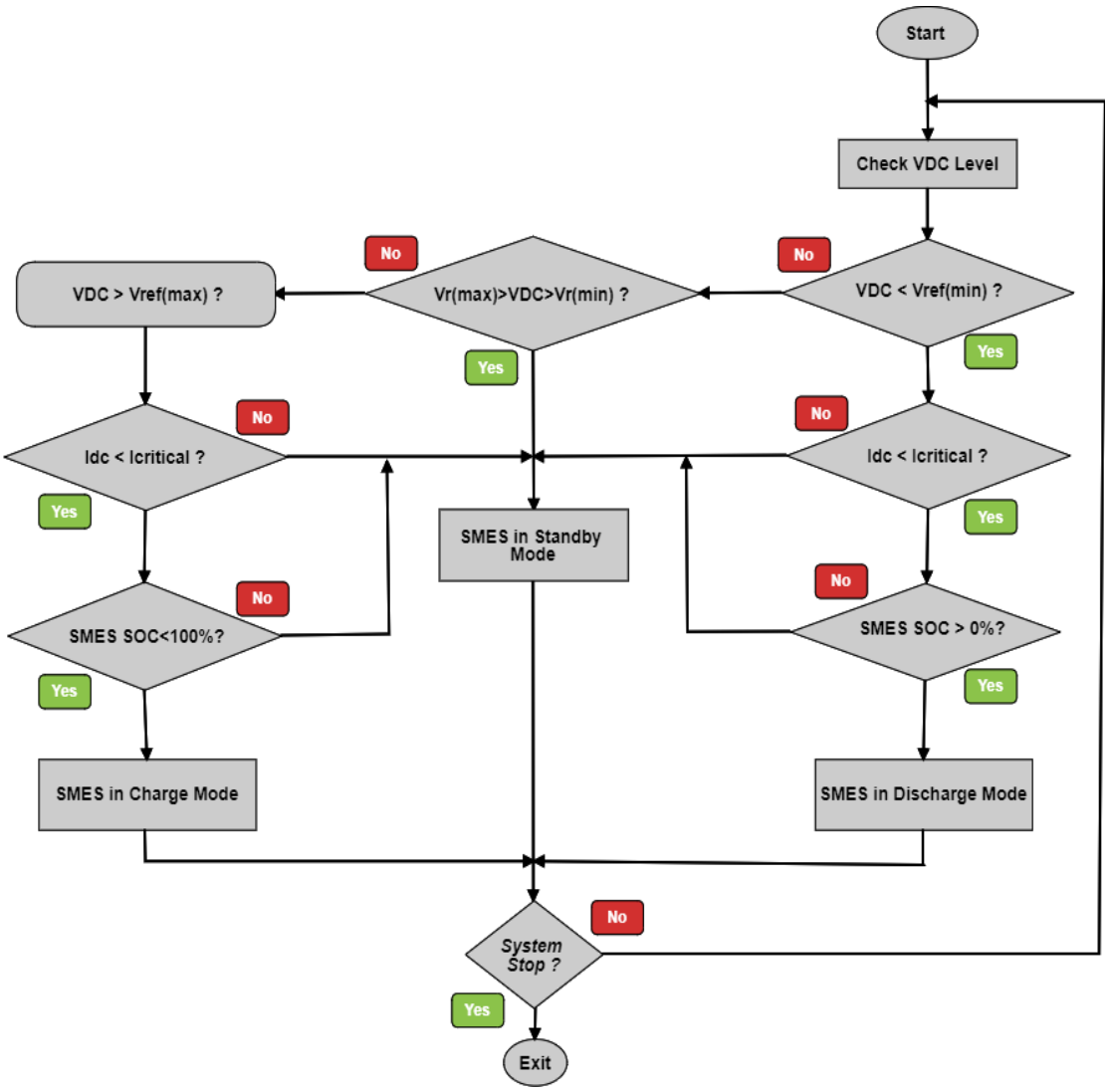


Figure 7.2: Flowchart illustrates the three modes of operation of SMES.

The inputs of the control system are the voltage of the DC bus (*VDC*), the current of the transmission line (*Idc*) and the current stored in SMES (*Ismes*), and the control system's outputs are d1 and d2 which are the pulses generated to control the IGBTs I1 and I2. $V_{ref(max)}$ is the maximum reference voltage which is 1.03 pu of the rated voltage in this study. $V_{ref(min)}$ is the reference minimum voltage which is 0.97 pu of the rated voltage in this study. SMES-SOC is the state of charge for SMES. If SMES-SOC is less than 100%, that means that the SMES is not fully charged and can absorb more energy. If SMES-SOC is greater than 0%, that means that the SMES is not fully discharged and

can discharge current to maintain the DC bus voltage at the reference point. Because the DC bus voltage drops in both the DC fault and the AC side during power loss, the two cases are differentiated by comparing I_{dc} (the transmission line current) to $I_{critical}$ (the threshold value of the CBs). If I_{dc} is higher than $I_{critical}$, the SMES should operate in the standby mode.

7.3 TeA final power system architecture and simulation results

After integrating SMES to the power system architecture, the final power system architecture is shown in Fig. 7.3. The system is subjected to two faults; 2 and 4 sec in the following two subsections.

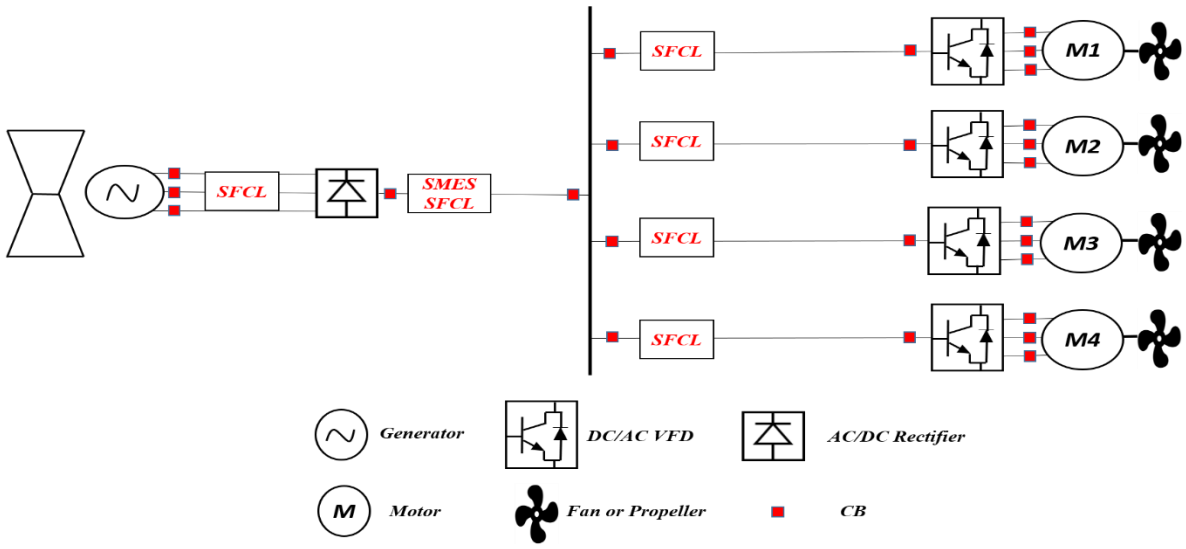


Figure 7.3: Final power system architecture for TeA.

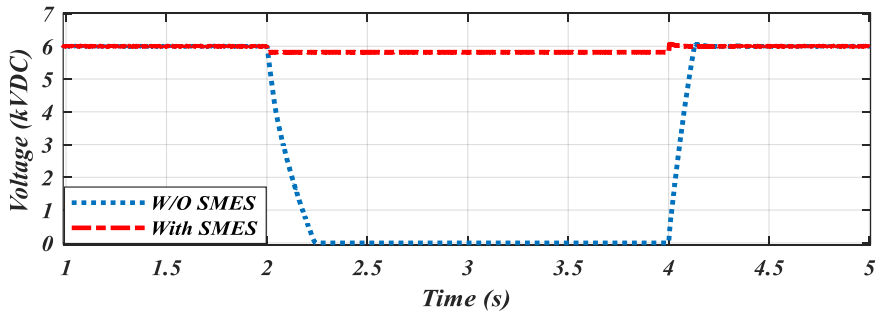
7.3.1 Case study #1

In this case study, the system is subjected to a temporary power loss for 2 sec. The SMES parameters, including capacity, weight, volume and inductance are shown in Table 7.1 to maintain the DC bus voltage for up to 2 sec. The weight and volume were estimated based on [167].

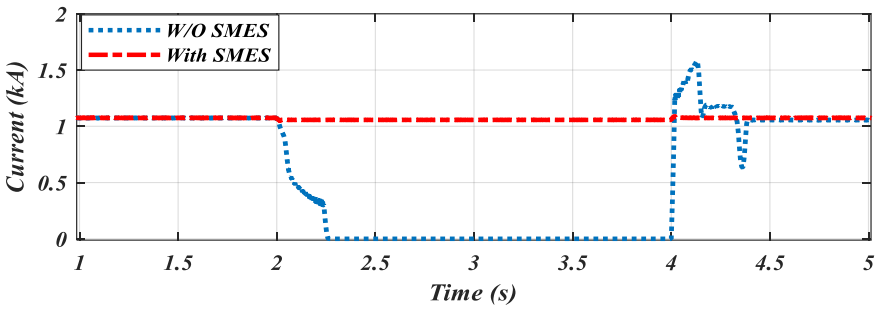
Table 7.1: SMES parameters for case study #1

Parameter	Value
SMES capacity (kWh)	3.819
SMES weight (kg)	477.37
SMES volume (m^3)	1.9
SMES inductance (H)	1.1

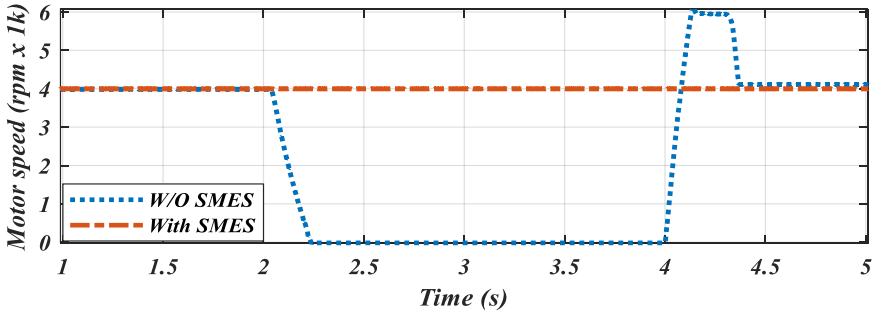
This system is subjected to power loss for two seconds, starting at t=2 sec. Fig. 7.4 (a) shows the DC bus voltage with and without the SMES device. The main transmission line current is shown in Fig. 7.4 (b) with and without the SMES device. The speed of the motor M4 is shown in Fig. 7.4 (c) with and without the SMES device. Finally, the SOC of the SMES is shown in Fig. 7.4 (d).



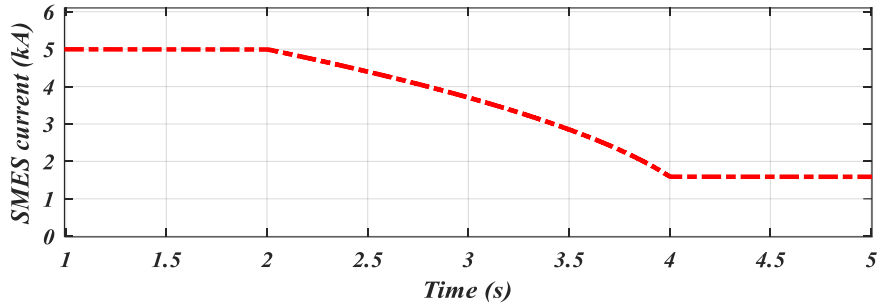
(a)



(b)



(c)



(d)

Figure 7.4: System behaviours with and without SMES during generator loss for 2 sec(a) DC bus voltage (b) current in kA (c) M4 motor speed (d) SMES current (kA)

When the system is subjected to temporary power loss, the SMES starts discharging to maintain the voltage at the minimum reference point which is 0.97 pu of the rated voltage, as shown in Fig. 7.4 (a). With the SMES, the current was maintained at the required current, thus maintaining the speed of the motor M4 at the required speed, as shown in Fig. 7.4 (b) and (c), respectively. Without the SMES, the current of the transmission line and the speed of M4 drops to zero within a few milliseconds. Fig. 7.4 (d) shows the SMES discharging current to feed the propulsion system during power loss.

7.3.2 Case study #2

In this case study, the system is subjected to a temporary power loss for 4 sec, starting at t=2 sec. The SMES parameters for case study #2 is shown in Table 7.2. The weight and volume were estimated based on [167].

Table 7.2: SMES parameters for case study #2

Parameter	Value
SMES capacity (kWh)	7.638
SMES weight (kg)	954.7
SMES volume (m^3)	3.819
SMES inductance (H)	1.518

The DC bus voltage, the main transmission line current and the speed of motor M4 with and without the SMES device are shown in Fig. 7.5 (a), (b), (c), respectively. Finally, The SOC of the SMES is shown in Fig. 7.5 (d).

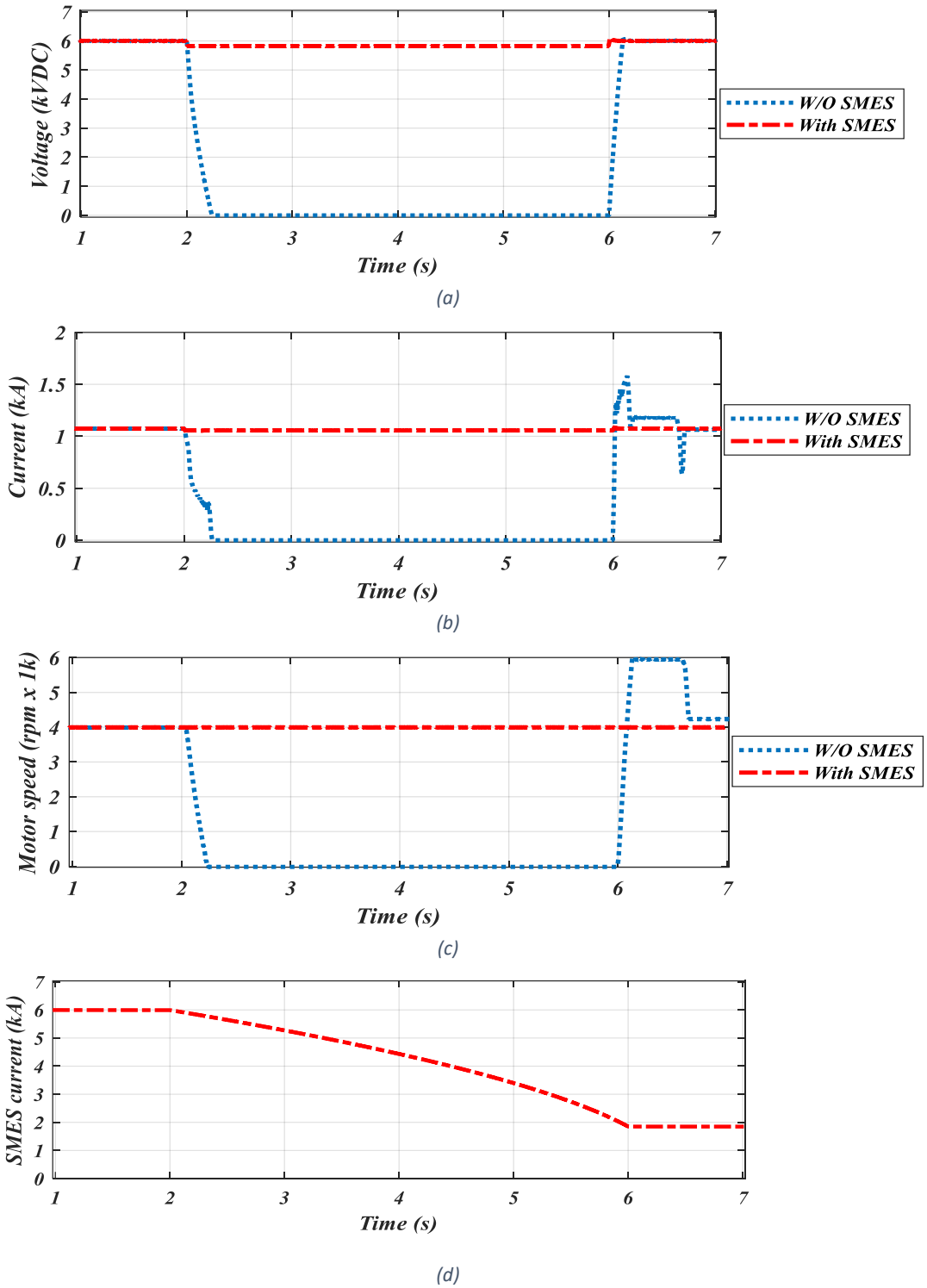


Figure 7.5: System behaviours with and without SMES during generator loss for 4 sec (a) DC bus voltage (b) current in kA (c) M4 motor speed (d) SMES current (kA)

The SMES's response to the temporary power loss for 4 sec is similar to the SMES's response in the 2 sec case study. The SMES device was able to discharge current immediately to maintain the DC bus voltage at the reference value (0.97 pu) and maintain the propulsion system speed at the required speed. However, the weight and size of SMES were larger and heavier than the SMES with the 2 sec case study. With a low energy density for SMES at 8 Wh/kg [167], SMES is not an ideal long-term energy source. However, as SMES has a high power density, with up to 2000 W/kg [167], SMES can be an excellent short-term power source that can be supported by another power source like a battery system. Designing a SMES/Battery hybrid energy storage for TeA is one of the goals of future work.

7.4 Chapter discussion and conclusions

The power generated by generators has several limits, including power limits, limits of the generator's active power, and ramp-rate limits. In addition, the generators may suffer from intermittent power loss. Adding SMES to the transmission line maintained the voltage, current and speed of the propulsion system for up to 4 seconds. The control of the system was demonstrated to work efficiently after losing AC-side power for up to four seconds. The capacity of the SMES in this study was calculated to supply the propulsion system for 2 and seconds during the cruise (1.5625 MW × 4).

However, SMES technology has not fully matured yet. In this study, the focus was only on the device's electrical performance within the proposed power system architecture. The design may need further investigation in terms of mechanical stress and Lorentz force. Additionally, the weight of the SMES is relatively high, considering it supports the system for short periods. However, a hybrid SMES/Battery system can be the solution to reduce the weight by exploiting the advantages of the high energy

density of the battery (250 Wh/kg) and the high power density of SMES (up to 2000 W/kg), thus increasing the overall energy density. Designing a hybrid SMES/Battery is one of the future work goals. More discussion of the SMES/hybrid energy storge for TeA is in the future work section.

Chapter Eight

8. Conclusions and Future Work

8.1 Summary

This thesis investigated the TeA power system and the behaviour of different kinds of faults within it. Because the fault currents were extremely high, a multilayer thermoelectric resistive SFCL has been modelled to mitigate the high fault currents and to ensure safe operation for the CBs. Additionally, a SMES with its control was integrated into the TeA power system to supply the propulsion system during short periods of power loss. The accomplished work/results are summarized as follows:

- One set of the airborne DC microgrid based on the NASA N3-X power system architecture, which includes one generator, one DC/AC VSC, transmission lines/connectors and four motors with their VFDs, has been modelled in MATLAB® /Simulink environment to conduct the DC fault analysis.
- The DC fault analysis has been carried out for two different voltage levels. The recommended range of DC bus voltage levels for the TeA power system architecture was found to be in the range of 4 – 10 kVDC. In this thesis, two voltage levels were modelled and used for the fault analysis: 6 kVDC and 9 kVDC.
- A multilayer thermoelectric r-SFCL has been modelled to reduce the fault currents. The thermal and electrical characteristics of each layer and the heat transfer coefficient were taken based on experimental work in the literature

review. The r-SFCL has been tested for 20 msec temporary faults under fault conditions with different copper stabilizers and shunt resistors.

- The best r-SFCL in terms of fault current limiting capability and recovery time was integrated into the TeA power protection system. Because the fault detection systems and the CBs operational time cause a time gap between the fault occurrence and fault clearance, the TeA power system was subjected to five faults with five different time gaps to showcase the impact of the r-SFCL on the protection system and its response.
- A SMES device with its control was integrated into the TeA power system architecture to supply the propulsion system during short periods of power loss of up to 6 sec.

8.2 Conclusions

The conclusions and achievements made were as follows:

- The results show that the fault currents were extremely high with pole-to-pole and pole-to-ground with low grounding impedance faults at both 6 and 9 kVDC. However, the fault currents are higher in the 9 kVDC system than in the 6 kVDC system by 23.24 % (in pole-to-pole fault), despite the smaller DC-link capacitors and higher line impedances in the 9 kVDC system.
- The fault analysis for the TeA power system architecture demonstrated two main challenges for the power system protection; an extremely high fault current with the pole-to-pole and pole-to-ground with low grounding impedance faults which is challenging to clear/isolate with traditional power protection practices and devices. The second challenge is a low fault current with the pole-

to-ground with high grounding impedance fault which, in some cases, is not detectable.

- The detection of the pole-to-ground with high grounding impedance fault was identified as one of the design challenges of the TeA power system based on the DC fault analysis. Different fault detection methods were used to determine the highest grounding impedance where the fault currents were still detectable. Based on the OC detection method, the highest grounding impedance where the fault currents were detectable was 1.07 Ω. Whereas with the CD detection method, the fault currents were detectable up to 6 Ω grounding impedance.
- Integrating r-SFCLs into the TeA power system supports the protection system by reducing the fault current, slowing the voltage drop at the main DC bus, and therefore improving the stability of the speed of the motors in the healthy feeders. Based on the results in chapter 6, the TeA power protection system offers better performance in terms of fault currents, voltage drop and motor speed stability with the 64 msec time gap and r-SFCLs compared to 4 msec without r-SFCLs.
- Finally, the SMES device showed a good capability to maintain the DC bus voltage at the required value and stabilize the propulsion system at the required speed, consequently improving the overall system's stability.

8.3 Limitations of the study

There are limitations to this study for several reasons, including the immaturity of some technologies which would have been used in this study, software limitations, or limitations of a feasible scope. The limitations of this study are as follows:

- Due to the relatively high cost of superconductor tapes and the large size of the SFCLs in this study, it was not currently possible to carry out the experimental work. This study was limited to show the performance of the SFCLs by the simulation tool (MATLAB/Simulink environment). However, an experiment set up to show the SFCL behaviours is part of the future work.
- The TeA power system architecture was proposed to be a complete superconducting network, including superconducting machines for generation units and propulsion systems, superconducting cables, SFCLs and SMES. However, because some of these components are still under development, this study was limited to SFCLs and SMES and their performance. In the future work section, this limitation will be discussed further.
- The DC fault analysis was conducted without considering the atmospheric pressure atmosphere of the aircraft system. Atmospheric pressure may have some effects on aircraft components and the materials used, and thus affect the fault analysis and fault behaviours, which means that there may be variations at different altitudes and in different locations. This needs further investigation.

8.4 Future work

With the concept still under investigation in the test phase, it is not feasible to address all network-related problems in a single study. With the considerable achievements made in the area so far, the next steps which would add value to the existing work should focus on solving the following major issues:

- As mentioned in the limitations of this study, this study was limited to show the performance of the SFCLs by simulation tool (MATLAB/Simulink environment). However, one of the main goals of the future work is to set up an experimental test for the SFCLs and compare the experimental results to the simulation results. In order to test the SFCL behaviour, a DC test rig will be built to generate DC faults. The DC fault behaviour is expected to be based on the simulation work. The SFCL device will be tested in terms of fault current limiting capability and recovery time.
- The TeA was proposed to be a complete superconducting network, as mentioned in the limitations of this study. However, because of the immaturity of some technologies, this study was limited to SFCLs and SMES behaviour in this power-dense electric network. One of the major milestones to be worked on is to design/model a complete superconducting network, thus improving upon the accuracy of this study. This can be achieved by integrating superconducting cables to the current TeA power system. Superconducting machines may also be integrated, depending on the maturity of existing machines and the availability of the necessary data to design such machines. This is considered as a long-term goal for future work.
- In this study, the multilayer thermoelectric r-SFCL was modelled/tested with copper stabilizers with different sizes. In future works, the r-SFCLs will be designed using different materials for the stabilizers, including stainless steel, and the impact of these different stabilizers on the behaviour of the SFCLs will be evaluated.
- Designing complete protection strategies for the TeA power system is one of the goals of future work. The protection strategies must ensure system

reliability and a high level of system resilience under any unexpected fault scenarios.

- A hybrid SMES/battery system can be designed to reduce the generator size and flatten the curve of the typical flight cycle, as the electric generators in TeA are typically sized for the take-off power rating, despite the fact that take-off takes up less than 20% of the total flight time. By taking advantage of the high power density of SMES and the high energy density of battery, a hybrid SMES/battery system can be used to reduce the size of generators, as the additional power required during take-off can be generated by the generators or transferred from another source prior to take-off.

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Appendix A; Paper #1

MT25-Wed-Af-Po3.07-05

Stability Improvement of DC Power Systems in an All-Electric Ship Using Hybrid SMES/Battery

Hamoud Alafnan, Min Zhang, Weijia Yuan, Jiahui Zhu, Jianwei Li, Mariam Elshiekh and Xiaojian Li

***Abstract*—As the capacity of all-electric ships (AES) increases dramatically, the sudden changes in the system load may lead to serious problems, such as voltage fluctuations of the ship power grid, increased fuel consumption and environmental emissions. In order to reduce the effects of system load fluctuations on system efficiency, and to maintain the bus voltage, we propose a hybrid energy storage system (HESS) for use in AESs. The HESS consists of two elements: a battery for high energy density storage and a superconducting magnetic energy storage (SMES) for high power density storage. A dynamic droop control is used to control charge/discharge prioritisation. Manoeuvring and pulse loads are the main sources of the sudden changes in AESs. There are several types of pulse loads, including electric weapons. These types of loads need large amounts of energy and high electrical power, which makes the HESS a promising power source. Using Simulink/Matlab, we built a model of the AES power grid integrated with a SMES/battery to show its effectiveness in improving the quality of the power grid.**

***Index Terms*—All-electric ship (AES), hybrid energy storage system (HESS), superconducting magnetic energy storage (SMES), pulse load.**

I. Introduction

As the world trending to be electric, ship technology is no exception. In the past, ship design did not depend mainly on the electrical power system because ships were propelled mechanically by connecting the steam engines or turbines directly to the propellers. However, the introduction of ships that were propelled electrically opened the door for the increased inclusion of electrical design in shipbuilding. To encourage the trend to electrification, the concept of all-electric ship (AES) was proposed by the U.S. Navy [1]. As the capacity of the AES is expected to reach hundreds of megawatts in the near future [2], a high-performance power system with multiple power sources is required to meet such huge power demands. The AES has different types of loads, including propulsion loads, ship service loads and pulse loads, such as electrical weapons. Electrical weapons rely on stored energy to attack targets, which need a high amount of power in a short period.

On the AES design, one of the most important features is the ramp-rate of the generators. The ramp-rate is the increased or decreased rate of the output power per minute and usually in MW/minute. The ramp-rate of ships' generators, such as gas-turbine generators are in the range of 35 to 50 MW/minute, whereas the pulse loads required a 100 MW/second ramp-rate, which is significantly higher than the ramp-rate of the generators [3], [4]. If the changes in the loads are faster than the ramp rate of the generators, unbalanced power between loads and generators occurs, which leads to instability in the power system. Because the ramp-rate of the ship's generators is not high enough to maintain the power demanded by electrical weapons, the need for an integrated power system (IPS) architecture is inevitable. The IPS is intended to provide the total amount of power required by the AES by using common set of sources [5]. Missions that require high power support, such as a weaponry system and improve the efficiency of propulsion, which are some of the advantages of the use of an IPS in ships [6]. IEEE 1709 recommends the use of medium-voltage DC (MVDC) in shipboard power systems, which improves the reliability, survivability and power quality of the system [7].

The hybrid SMES/Battery has been proposed for railway substations by using fuzzy control [8]. The use of the SMES was proposed in a hybrid vehicle in which a cryogenic tank already existed [9]. A SMES/Battery hybrid energy storage system (HESS) was integrated into microgrids to mitigate the influence of the renewable generations [10]. The implementation of a HESS for AESs has been proposed to supply both the peak and pulsed loads. Several studies were performed to mitigate the effects of the pulse loads on shipboard power system by using HESS. A supercapacitor and batteries were combined to supply pulse loads and support grid stability with different control schemes [11], [12]. A flywheel energy storage system was added to the system to maintain the health of the ship's power systems by maintaining the propulsion motor speed and the generator speed during pulse load periods [13].

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In this paper, we propose the use of the superconducting magnetic energy storage (SMES)/battery HESS in AESs. Compared with supercapacitors, flywheels, and other energy storage devices, SMES devices have higher power density, faster time response and unlimited charge and discharge life cycles [14], [15]. Because the battery has a relatively low power density [16], it cannot respond quickly in supplying the high transient current that is needed for the pulse loads. In this model, SMES works as a high power density device and a battery as the high energy density device. A dynamic droop control is used to coordinate the charge/discharge prioritisation between the SMES and the battery. The ultimate goal of the HESS, based on dynamic droop control, is to supply the power demanded by the pulse loads and to maintain the main DC bus voltage within the targeted range.

II. Model Analysis

The MVDC power system on ships recommended by IEEE 1709 [7] was chosen to be the platform for testing the performance of the system and to assess the efficiency of the dynamic droop control. The simplified AES is shown in Fig. 1. The power on the ship is generated by two generators that meet the installed power demands. The two generators are connected to the main DC bus via AC/DC receivers. The two generators provide the power to the load evenly. Different types of loads are installed in the AES, including the propulsion load, ship service loads and pulse loads. In this model, the pulse loads represent the electrical weaponry system. The HESS is added to the system to supply the pulse loads. A dynamic droop control is used to arrange the charge/discharge in different energy storage devices.

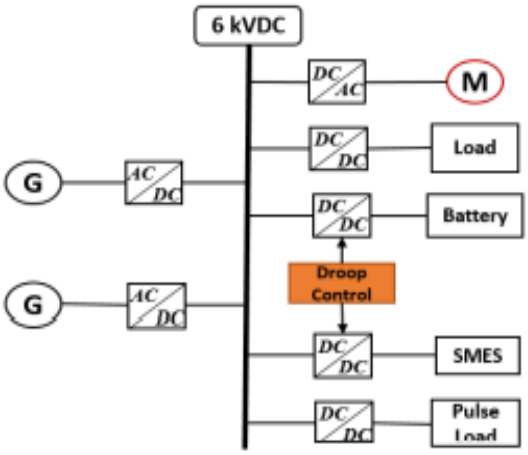

Fig. 1. Simplified AES including HESS.

A. On-board Power Generation

There are several constraints on power generated by generators, including power equilibration limits, limits of the generator's active power, and the ramp-rate limits [17], [18]:

$$\sum_{j=1}^{G} P_{ij} = P_{Di} + P_{Li} \quad i = 1,2,\dots,N \tag{1}$$

$$P_j^{min} \le P_{ij} \le P_j^{max} \quad i = 1,2,..,N, j = 1,2,\dots,G \tag{2}$$

$$\frac{P_i(n) - P_i(n-1)}{\Delta t} \le k \tag{3}$$

where P_j^{min} and P_j^{max} are the upper and lower allowable active power outputs of generator j, respectively. $P_i(n)$ and $P_i(n-1)$ are the output power of the generator in two different moments Δt, and k is the allowable ramp-rate of the generator. Because the pulse load requires a high amount of power in a short period, and the ramp-rate of the generator cannot maintain it, the HESS is implemented in the system to supply this load. In our model, two diesel generators, 7 MW, 6.6 kV and 50 Hz, are modelled to generate power for the simplified AES.

B. Electric Propulsion Motor

In this system, a synchronize motor is used as the electric propulsion motor. The propeller is connected directly to the synchronize motor. The mechanical load power of the motor is represented in (4):

$$P_{mec} = 2\pi nQ \tag{4}$$

where n represents the propeller rotational speed and Q is the torque of the propeller. The relationship between the supply frequency and the motor speed can be expressed as:

$$n = \frac{120 f_r}{P} \tag{5}$$

where n represents the propeller rotational speed, f_r is the supply frequency and P is the number of motor poles. The power capacity of the propulsion motor is 2800 hp (≈ 2 MW).

C. Hybrid Energy Storage System

Because the ramp-rate of the generator is not high enough to supply and maintain the power demands of pulse loads, energy storage systems (ESS) have become essential to increase the amount of energy delivered within a short period. Two types of energy storage devices were chosen for this design: SMES and lithium-ion batteries. SMES is used as the high power density device to support the system during the transient periods. The SMES is controlled to deal with the short-term energy deficiency. The stored energy of SMES is calculated as follows:

$$E_{smes} = \frac{1}{2} L I^2 \tag{6}$$

Lithium-ion batteries are implemented in the AES to deal with long-term energy deficiency. Compared with other types of batteries, lithium-ion batteries have better energy density, low self-discharge and high efficiency [19], [20]. To protect the battery from overcharging and deep discharging, the state of charge (SOC) of the battery is regulated between 30% and 90% [21].The design of the battery and SMES are based on the ship loads. There are three different types of load on the AES; 7 MW static load (ship service load), 2 MW motor load and 5 MW pulse loads. During the normal operation, the ship service load and the motor load are applied to the system with a total power demand of 9 MW. During the pulse load periods, the demand rises by 5 MW to a total of 14 MW. The battery capacity is

calculated by (7) at 13.88 kWh to cover the requirements of the pulse loads demand and to maintain the battery SOC constraints.

$$Battery_{Cap} = \frac{Pulse\ loads * time\ (hour)}{SOC - (Upper\ Cont. + Lower\ Cont.)} \quad (7)$$

Because the SMES is more expensive than the Lithium-Ion battery in terms of energy density [19], the goal was to minimize the SMES size as much as possible whilst maintaining the voltage level at 6 kVDC. It was found that when the SMES size is reduced to < 500 kJ, a voltage drop occurred in the main DC bus before the battery began discharging. The design parameters of the AES are summarized in Table I.

TABLE I
THE DESIGN PARAMETERS OF THE AES

Parameter	Quantity	Value
Generator	2	7 MW, 6.6 kV, 50 Hz
Motor	1	2800 hp (= 2 MW), 6.6 kV
Battery	Battery Bank	13.88 kWh, 92.53 kg, 0.0694 m^3 [22]
SMES	1	500 kJ (= 138.8 Wh), 17.35 kg, 0.69 m^3 [22]

III. ENERGY STORAGE CONTROL METHOD

The main goal of this work is to design a dynamic droop control system to operate the HESS at better efficiency during pulse load periods. Previous studies demonstrated the droop control used to share different power sources [23], [24]. This paper proposes the use of HESS based on dynamic droop control to take advantage of the high power density of SMES and the high energy density of the battery in order to mitigate the effects of the pulse loads on the system's stability. The main principle of the control strategy is to generate different pulses in the SMES converter to control the charge and discharge of the SMES. The battery is controlled by a PI controller, which compares the main bus voltage and the voltage reference and considers the SOC of the battery. When the pulse load is added to the system, the SMES discharges immediately to feed the load and maintain the main bus voltage. Based on the dynamic droop control, the SMES discharge rate will decrease gradually to allow the battery to increase the discharge rate based on the pulses that are generated to the SMES and the battery. The main DC bus voltage is maintained within the required range ($Vref(min) < Vbus < Vref(max)$). According to the IEEE standard [7], the DC voltage tolerance limits should be ± 10%. However, the tolerance limit was tightened to ± 3% in order to improve the system stability, as this was the main concern of this study. $Vref(min)$ is 0.97 pu of the nominal voltage, and $Vref(max)$ is 1.03 pu of the nominal voltage.

A. The SMES DC/DC Controller

The H-bridge DC/DC converter is used to control the charge and discharge of the SMES. It consists of two diodes (D1, D2), two MOSFTs (M1, M2) and an output capacitor, as shown in Fig. 2. There are three operation modes: the charge mode, the discharge mode and the standby mode. The charge/discharge rate of the SMES is not only controlled by $Vref$, but also controlled by the amount of the current stored in the SMES by (8) and (9). The goal of this control method is to change the charge and discharge rates of SMES based on the amount of the current stored in SMES to avoid the sharp charging and discharging. When SMES current decreases the discharge rate of the SMES decreases by (9), the voltage drop in the main DC bus slow down, thus the battery bank has more time to discharge to maintain the main DC bus at the required level. The three operation modes are shown in Fig.2.

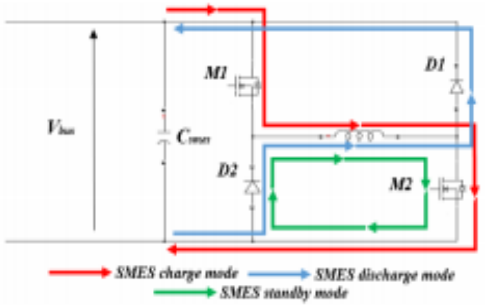

Fig. 2 The DC/DC H-bridge converter of SMES with three operation modes.

1) ($V_{bus} > V_{ref(max)}$) Charge mode

In charge mode, as shown in Fig. 2, the red directional arrows indicate that d1 (the duty ratio of M1) and d2 (the duty ratio of M2) are on, allowing the SMES to charge. At the same time, d1 receives another pulses according to (8) in order to decrease the charge rate of SMES gradually, allowing the battery to charge quickly. The two pulses are connected by the AND logical function, as shown in Fig. 3.

$$q = (k_a)\, exp(\frac{I_{smes}}{k_{smes}})^{k_b} \quad (8)$$

Where I_{smes} is the amount of the stored current in SMES, k_a, k_b and k_{smes} are adjustable parameters that control the transition period between SMES and the battery based on I_{smes}.

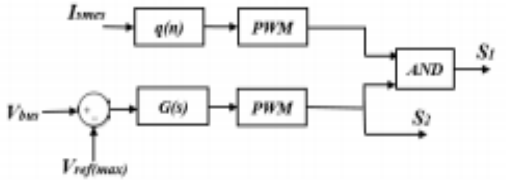

Fig. 3. Block diagram of the H-bridge DC–DC converter controller (charge mode)

2) ($V_{bus} < V_{ref(min)}$) Discharge mode

In discharge mode, d1 and d2 are off, allowing SMES to discharge through the two diodes as shown by the blue path in Fig. 2. At the same time, d2 receives another pulses, according to (9), to decrease the discharge rate of SMES gradually, allowing the battery to discharge quickly. The two pulses are connected by the OR logical function, as shown in Fig. 4.

$$q_2 = (k_a)\, log_{10}(\frac{I_{smes}}{k_{smes}})^{k_b} \quad (9)$$

Where I_{smes} is the amount of the stored current in SMES, and k_a , k_b and k_{smes} are adjustable parameters that control the transition period between SMES and the battery based on I_{smes}.

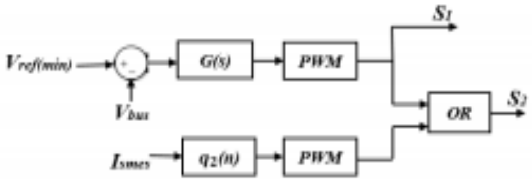

Fig. 4. Block diagram of the H-bridge DC–DC converter controller (discharge mode).

3) ($V_{ref(max)} > V_{bus} > V_{ref(min)}$) Standby mode

In standby mode, the bus voltage is in the acceptable range between 0.97 and 1.03 pu of the nominal voltage. Hence, no output current from SMES is needed. To keep the current circulating between D2 and M2, d1 is off and d2 is on.

B. The Battery DC/DC Controller

The half bridge DC/DC bidirectional converter based on the PI controller is used to control the battery charge and discharge. The converter consists of two IGBTs, Q1 and Q2, as shown in Fig. 5.

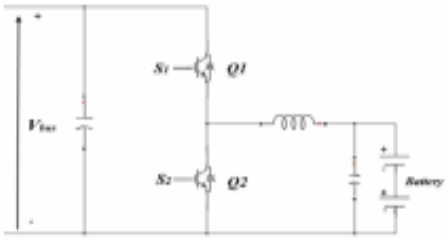

Fig. 5. DC/DC bidirectional converter based on PI controller.

In this control technique, the main DC bus voltage is compared with the reference voltage *Vref* as shown in Fig.6. The PI controller allows the battery to increase and decrease the charge and discharge rates based on the SMES current rate. When the SMES current starts to decrease by the dynamic droop control, the voltage starts to decrease slightly and the PI controller allows the battery to discharge and maintain the power demanded by the pulse load. The controller maintains the battery's SOC between 30% and 90%. More details pertaining to the battery DC/DC controller, the circuit and the control challenges can be found in [25], [26].

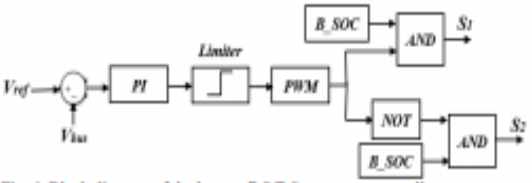

Fig. 6. Block diagram of the battery DC/DC converter controller.

IV. Simulation Results and Discussion

The simplified AES shown in Fig. 1 is modelled in the SimPowerSystems™ environment. The simulation results showed three different kinds of system behaviour: without ESS, with battery only and with HESS.

The simulation results demonstrated that the HESS based on the dynamic droop control showed good performance during pulsed load periods, maintaining the main bus voltage at the required range and keeping the motor at the targeted speed. The system was subjected to pulse loads between t=4.0–7.0 s and between t=10.0–13.0 s. With the HESS, the minimum total generators capacity is 9 MW. However, without the HESS the minimum total generators capacity is 14 MW. The voltage of the main DC bus was 6 kVDC according to the IEEE standard [7].

In the conditions of without ESS and with battery only, when the pulse load was applied to the system at t=4.0 s, the voltage dropped immediately to almost 3 kVDC. In the battery-only system, because the battery fed the pulse load, the voltage was regulated to the targeted level within a short period. However, in the HESS condition, the voltage remained stable at the targeted level throughout the test, both with and without pulse loads. In contrast, when the pulse load was removed at t=7.0 s, the voltage increased rapidly because of the overcurrent. However, at the HESS, because the SMES absorbed the excessive current, the voltage stayed at the targeted level. Fig. 7 shows the comparison of the main DC bus voltage without ESS, with batter-only and with HESS.

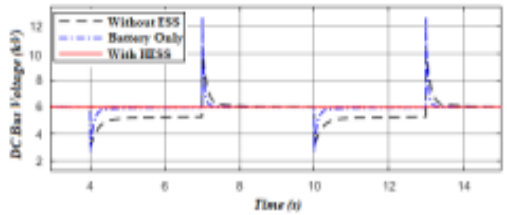

Fig. 7. The DC bus voltage without ESS, battery only system and with HESS.

Because the HESS was controlled to supply the pulse loads, the output power of the generators stayed constant at 9 MW with and without the pulse loads, as shown by the red line in Fig. 8.

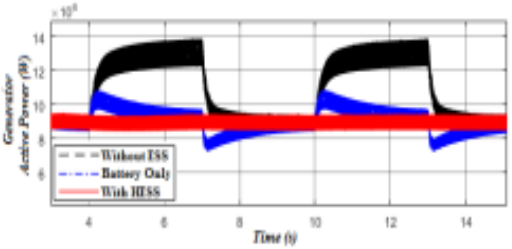

Fig. 8. The total power generation without ESS, with battery only and with HESS.

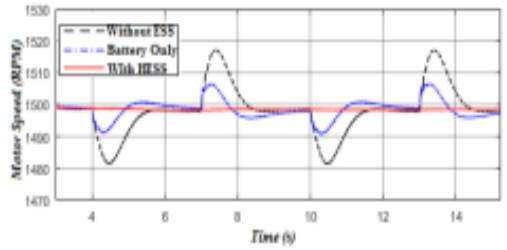

Fig. 9. The propulsion motor speed without ESS, with battery-only and with HESS.

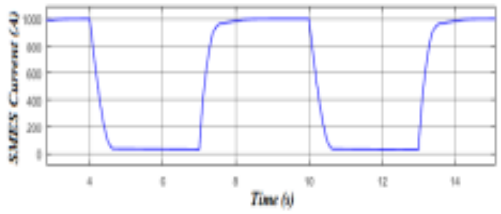

Fig. 10. SMES current.

In Fig.10, the maximum stored current in SMES is 1000 A. When the pulse load is applied to the system, SMES discharges immediately. It discharges 1000 A in 300 millisecond with a ramp-rate current of 3.3 kA/s. Because the discharge rate is controlled by both *Vref* and *Ismes*, the discharge rate is decreased when SMES current decreased by (9). The goal of decreasing the discharge rate of SMES is to slow down the voltage drop in the main DC bus, thus giving more time for the battery to responds. Fig.11 shows the battery current. When the pulse loads are applied to the system, the SMES and the battery discharge to meet the sudden change loads demand at the beginning, then the battery becomes the main source of the power after SMES completely discharged. The current ramp-rate of the battery is 2.6 kA/s and the constant discharge current is 800 A. In special electrical applications, such as pulse load applications there are a few electrical devices that can supply high power in a short period, such as SMES and batteries. The Lithium-Ion batteries current ramp-rate can be reduced by increasing the size of SMES. However, a trade-off between the cost of the SMES and the battery life must be made. In future work, an optimization study will be done to find the optimum battery vs SMES size to have the best price for the ESS and battery life. In this work the main goal is to study the performance of the HESS and the energy storage control method under the sudden load changes.

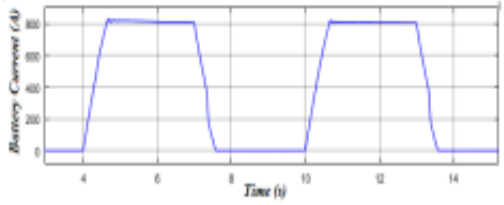

Fig. 11. Battery output current.

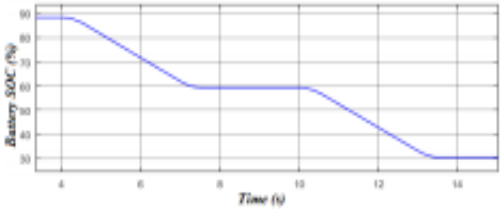

Fig. 12. Battery state of charge.

V. Conclusion

This paper proposes the use of the SMES/battery HESS based on the dynamic droop control in the AES to mitigate the effects of the sudden load changes on the system's stability. The AES including SMES/battery was built in the SimPowerSystems™ environment to test the system's behaviour with and without HESS. The HESS based on dynamic droop control showed good performance during the pulse load periods. By supplying the pulse loads from the HESS, the system maintained the voltage at the targeted level, keeping the motor at the required speed and maintaining constant generation output power both with and without pulse loads. To further investigate this approach, an experimental system containing a SMES and battery HESS will be constructed and tested in our laboratory. An optimization study for the SMES size and the battery life will also be performed.

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Appendix B; Paper #2

Application of SMES-FCL in Electric Aircraft for Stability Improvement

Hamoud Alafnan, Mariam Elshiekh, Xiaoze Pei, Shadan Altouq, Seyed Mahdi Fazeli, Qixing Sun, Min Zhang, Weijia Yuan

***Abstract*— The increase in aircraft passengers and airfreight traffic has given rise to concerns about greenhouse gas emissions for traditional aircraft and the resulting damage to the environment. This has led several companies and organizations, including NASA, to set goals to enhance aircraft efficiency as well as reduce fuel burn, pollution, and noise for commercial aircraft. The most notable electric aircraft (EA) concept is the N3-X, which was developed by NASA to achieve environmental goals while maintaining the annual growth of the aviation industry. However, one of the main challenges that EA facing is their overall weight. This paper proposes and explores an improved power system architecture for use in EA based on the N3-X concept. The number of superconducting magnetic energy storage (SMES) and fault current limiter (FCL) devices required can be reduced by utilizing multifunctional superconducting devices that combine the functionalities of both a SMES and a FCL, thus reducing the weight and cost of the EA by eliminating a complete device. The proposed control technique offers greater flexibility in determining the appropriate size of coils to function as a FCL, based on the fault type. The proposed EA power system architecture including the SMES-FCL devices is modelled in Simulink/Matlab to test the system performance under different failure scenarios.**

***Index Terms*——Electric aircraft (EA), fault current limiter (FCL), superconducting magnetic energy storage (SMES), turboelectric distributed propulsion system (TeDP).**

I. Introduction

TRANSPORTATION and electricity generation are the largest sources of carbon dioxide (CO_2) emissions in the US, at 34% per each, 68% in total [1]. The annual increase in aircraft passengers is estimated to be 6.5%, while the annual freight traffic growth rate is 4.4% [2], meaning that with current aviation transportation technology, CO_2 emissions will continue to increase dramatically. Because concerns about global warming and pollution are increasing, many companies and organizations have set goals to limit atmospheric pollution and greenhouse gas emissions, such as the National Aeronautics and Space Administration (NASA) and the Advisory Council for Aviation Research and Innovation in Europe (ACARE). The NASA and ACARE environmental goals relative to year 2000 are shown in Table I [3], [4]. As can been seen in Table I, the targeted improvements for both NASA N+3 and ACARE 2050 are extremely high, whereby reductions of CO_2 by 75%, NO_x by 90%, and external noise by 65% are infeasible in traditional aircraft design (gas turbine or piston engine) due of the relatively low efficiency ~ 40% [5]. To achieve such goals, the aircraft, including the propulsion system, must work with superior efficiency.

TABLE I
NASA AND ACARE ENVIRONMENTAL GOALS

Category	ACARE 2020	ACARE 2050	NASA N+2 ~2020	NASA N+3 ~2030
CO_2 reduction	50%	75%	-	-
NO_x reduction	80%	90%	75%	80%
Ex. noise	50%	65%	-42 dB	-71dB
Fuel burn	50%	-	50%	60%

The most notable EA concept is the N3-X, which has a range of 22.5 MVA for passenger aircraft and was proposed by NASA's Research and Technology for Aerospace Propulsion Systems (RTAPS) [6]. The N3-X combines the advantages of a turboelectric distributed propulsion system (TeDP), boundary layer ingestion (BLI), and superconducting technology to achieve the highest possible efficiency with the minimal weight. The N3-X power system architecture, known as the Inner Bus Tie Concept (IBTC), consists of four generators that supply 16 propulsors throughout a DC microgrid to give the required thrust.

However, there is a possibility that short fault currents may occur when this system is employed in larger passenger aircraft due to significant in-flight vibration or adverse weather conditions. Such occurrences may consequently cause serious permanent faults that can, if not properly addressed, lead to onboard fire, power disruption, system damage, or catastrophic failure [7],[8].

In the N3-X concept, NASA proposed the use of superconducting fault current limiter (SFCL) and superconducting magnetic energy storage (SMES) devices. A SFCL provides very effective current limitation within a few milliseconds [9]–[11]. which can offer a solution to the issue of short fault currents. SMES devices have a higher power density, faster time response, and unlimited charge and discharge lifecycles compared to other energy storage technologies [12],[13]. Such advantages are important for EA performance, where system reliability is a crucial point.

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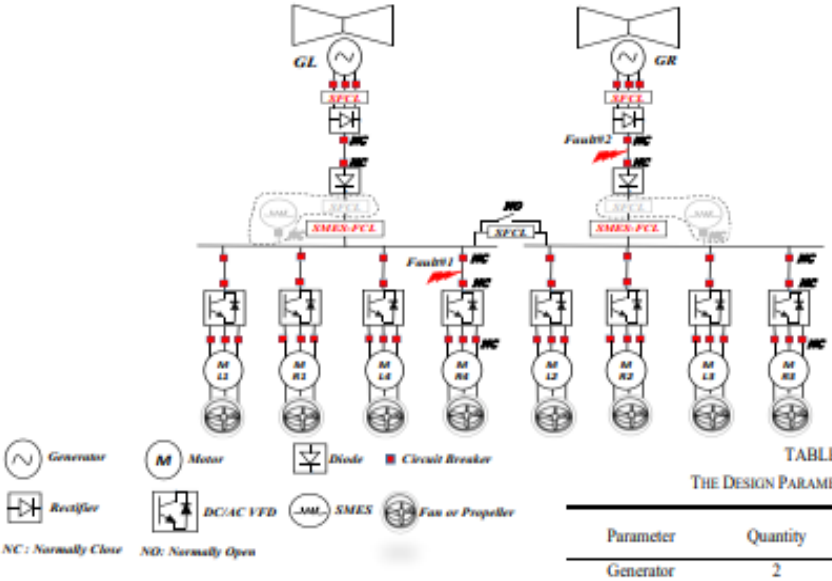


Fig. 1: Improved power system architecture based on N3-X

This paper proposes the use of a multifunctional superconducting device that can be used as both a SMES and FCL in EA, by using the same coils for the two modes, the SFCL devices with their components are eliminated as shown in Fig. 1. The elimination of a complete device can reduce the overall weight and cost of the EA. The proposed control algorithm allows the superconducting coils to work as a SMES or part of the coils as a FCL, based on the fault type. Multipurpose superconducting coils have been proposed in several applications, including in wind farms for AC and DC networks [14],[15]. For a DC network, previous work has suggested the use of the whole coil as a SMES or a FCL. However, the proposed control technique offers greater flexibility to determine the appropriate size of the coils to work as an FCL based on the fault current. The proposed power system architecture, including the control algorithm, is modelled and tested under different fault scenarios using the Simulink/Matlab environment.

II. System Description

The N3-X TeDP power system architecture, the Inner Bus Tie Concept (IBTC), proposed by NASA [16], was chosen as the platform for testing the performance of the SMES-FCL devices under various fault scenarios. The system components are shown in Table II.

The capacities of the generators, motors, and converters are based on the data of the aircraft proposed by NASA [16]. The SMES-FCL device capacity is calculated to supply a set of four motors for 320 ms at a cruise rated power of 1.5625 MW per motor. The propulsion system is required to produce 22.5 MW for maximum thrust during take-off [17].

TABLE II
The Design Parameters of the EA

Parameter	Quantity	Value
Generator	2	14.91 MW, 6 kV (GR-2, GL-2)
	2	7.46 MW, 6 kV (GL-1, GR-1)
Motor	16	1.86 MW
Converter, AC/DC	2	14.91 MW
	2	7.46 MW
Converter, DC/AC	16	1.86 MW
SMES-FCL	4	2 MJ (=0.556 kWh)

Because each motor can produce 1.86 MW thrust, at least 12 motors are required to work at the same time to ensure a stable operation. The voltage DC-link is rated at 6 kVDC, as recommend by NASA [18]. The multifunctional superconducting devices can replace the SMES and SFCL devices, which helps to reduce both the weight and cost of the EA while maintaining the same performance. In this paper, half of the power system architecture of the N3-X has been modelled, with eight motors (1.86 MW) and two generators (14.91 MW) as shown in Fig. 1, instated of the full sixteen motors and four generators [16].

A. SMES-FCL Device.

Due to its fast response, a SMES works well to maintain the voltage at the DC-link and ensures a stable operation for the propulsion system, which is a crucial for the EA design. SMES devices have been proposed and used in several applications, including a hybrid vehicle, electric ships, and microgrids [19]–[21]. The stored energy of a SMES is calculated as follows:

$$E_{smes} = \frac{1}{2} L I_{SMES}^2 \qquad (1)$$

where L is the inductance in Henry, I_{SMES} is the current stored in the SMES, and E_{smes} is the stored energy in SMES in Joule.

Resistive type superconducting fault current limiters are considered self-recovery devices. When the current passing through the SFCL coils exceeds their critical current, the SFCL resistance starts to increase dramatically, according to the following equation [22]:

$$\rho_{HTS} = \frac{E_c}{J_c(T)} \left(\frac{J}{J_c(T)}\right)^{N-1} T < T_c\,, \quad J > J_c \qquad (2)$$

where Ec = 1μV/cm is the critical electrical field. The N value is usually between 21 and 30 for Yttrium Barium Copper Oxide (YBCO) tapes. When the applied current is greater than the critical current, a joule heating effect occurs due to the exponential rise in ρ_{HTS}, leading to a rise in the temperature of the superconducting material.

$$J_c(T) = J_{co}\left(\frac{(T_c - T(t))^{\alpha}}{(T_c - (T_o)^{\alpha}}\right) \qquad T < T_c \qquad (3)$$

where α is 1.5, which is applicable to YBCO superconducting materials, J_{co} is the critical current density at the initial temperature T_o. As the current density $J_c(T)$ is less than the critical current density J_{co}, the coils' resistance will be neglected. However, when the current passing through the coils exceeds the critical current, the coils resistance starts to increase and limits the high fault currents. The concept of the resistive type SFCL is used to limit the fault currents in the EA system using the SMES coil.

The SMES-FCL device provides the two types of operation by using the same coils. For the SMES operation mode, the whole coil can be used to achieve the highest energy capacity. However, a few pancakes will be enough to achieve the desired limitation without affecting the system stability or the coil itself. In this study, a resistance value of 2 Ω is used as the fault current limiting resistance.

The SMES coils comprise 67 pancakes with an inductance of 1.005 H and a current rating of 2 kA. The SMES capacity is calculated by (1) to be 2 MJ [23],[24]. With regards to YBCO material containing copper stabilizer, it is possible to achieve a resistance value of 2 Ω through the use of two pancakes, whereby each one consists of 50 m of superconducting tape. If it were wound into a single pancake structure with an inner diameter of 10 cm and width of 4 mm, this particular design would correspond to an inductance of approximately 15 mH [14],[25].

B. Electric Propulsion Motor.

In this system, surface permanent magnet synchronous motors (SPMSM) are used as the electric propulsion due to the high power density and high efficiency [26]. The power capacity, number of pair poles, and nominal speed of each propulsion motor is 1.86 MW, 4, and 4000 rpm, respectively.

The principle of controlling the motors is based on the Field Oriented Control (FOC) strategy [27], as shown in Fig. 2. To implement the FOC strategy, the control unit translates the stator variables (currents) into a d-q frame coordination based on the rotor position as well as to compare the values with the reference values (ω_{ref}, i_{qref} and i_{dref}), and updates the PI controllers. The inverter gate signals are updated after the back transformation of the new voltage references into the stator frame coordination and compared with the modulating signals. In order to achieve the Maximum Torque Per Ampere (MTPA) strategy, i_{dref} is set to zero for the whole time [28] and the gains of all PI blocks have been fine-tuned by control theory analysis together with trial and error adjustments. In Fig. 2, S1-S6 are insulated-gate bipolar transistors (IGBTs) with integrated, anti-parallel diodes.

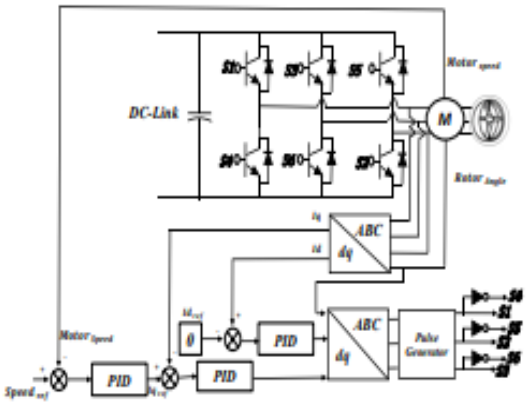


Fig. 2: Field Oriented Control (FOC) for an electric propulsion motor.

III. SMES-FCL Control Method

The multifunctional superconducting coils are designed to work in two different operation modes based on the fault position. If the fault occurs on the propulsion side, as is the case in Fault #1, part of the superconducting coils work as a FCL to limit the fault current and the rest of the coils are isolated to protect them from the overcurrent. However, if the fault occurs on the generation side, as is the case in Fault #2 in Fig.1, the superconducting coil works as a SMES to maintain the speed of the propulsion system and the voltage at the DC-link.

The SMES-FCL device is programmed based on the current and the voltage measurements on the DC bus. If the fault occurs at the generation side as in Fault #2, both the current and voltage on the DC bus drop; as a result, the SMES-FCL works as a SMES in discharge mode, as shown in Fig. 3 (a). During the normal operation, the switches, S1, S4 and S5 are closed, S2, S3 and S6 are open. When the SMES-FCL works in SMES operation mode, the switches I1 and I2 control the discharge rate of the SMES based on the control algorithms which allow the two switches to discharge the appropriate amount of current to maintain the DC-link voltage at the acceptable level and the motor speed at the reference speed.

If the fault occurs on the propulsion side as in Fault #1, the current increases dramatically and the DC bus voltage drops. In this case, the SMES-FCL works as a FCL to limit the fault current and isolate the rest of the coils for protection, as shown in Fig. 3 (b), whereby two pancakes are used as a FCL, as shown by the red arrows, and the rest of the coils are isolated for protection, as shown by the green arrows. For the FCL mode, the switching sequence is: I1 is off and I2 is on to put the coils in the standby mode. Then, S2, S3, and S6 are closed to isolate the SMES coils for protection. Finally, S1, S4 and S5 are opened to force the current to go through the two pancakes which is the FCL part to limit the fault current. In Fig. 3, S1-S6 are unidirectional, reverse blocking IGBTs. More details pertaining to controlling I1 and I2 in the SMES mode can be found in [20]. Fig. 3 (c) shows the SMES charging mode of the SMES-FCL, and Fig. 3 (d) shows the SMES standby mode.

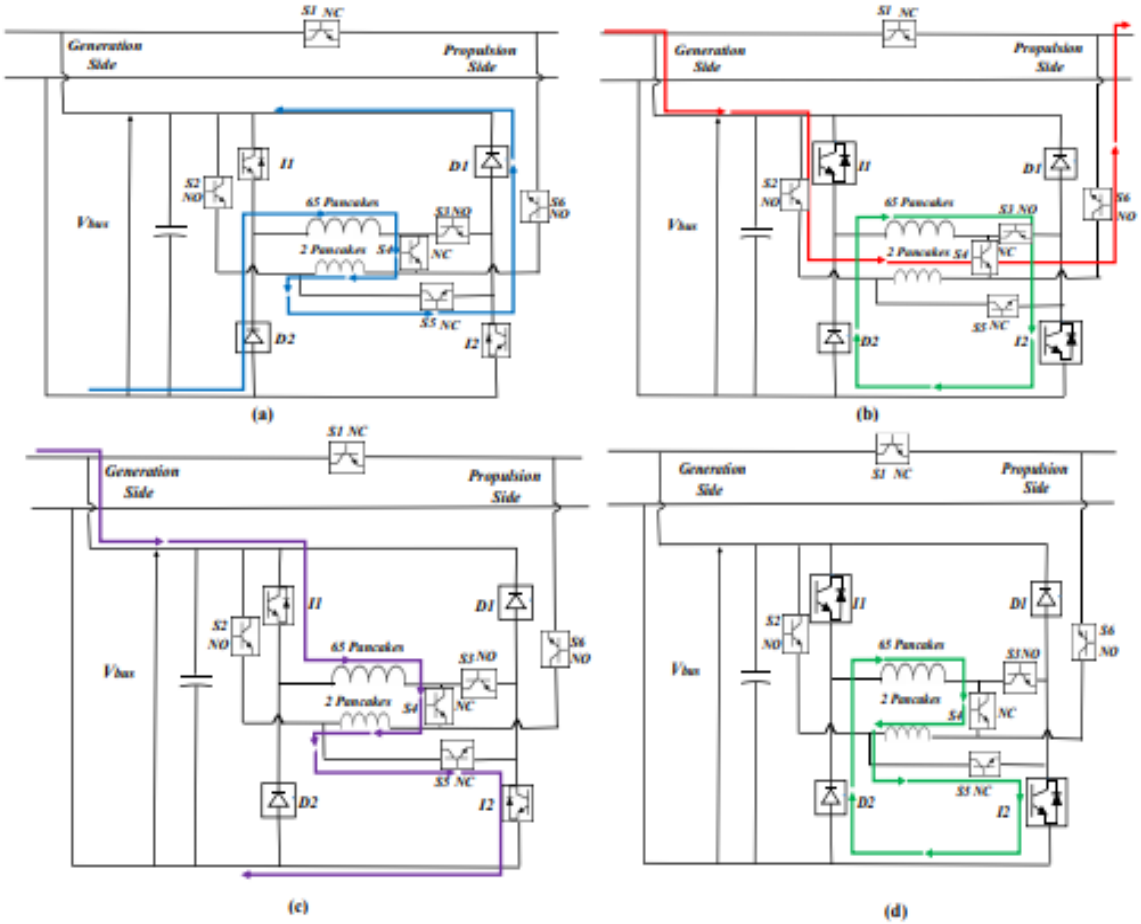


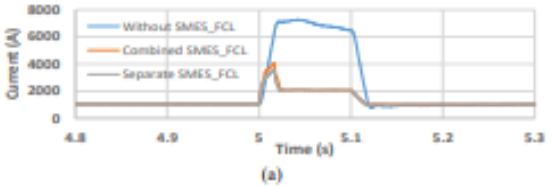
Fig. 3: SMES-FCL control topology, (a) SMES discharge mode, (b) FCL mode, (c) SMES charge mode, and (d) SMES standby mode.

IV. Simulation Results & Discussion

The power system architecture of the EA shown in Fig. 1 is modelled in the SimPower™ Simcape™ systems environments to test the performance of the SMES-FCL devices under different fault scenarios. Based on the control topology, Fault #1 made the SMES-FCL device work in the FCL mode, while Fault #2 made the SMES-FCL device work in the SMES mode. To show different types of DC faults in the DC microgrid of the EA, a pole-to-pole and pole-to-ground faults are applied at the location of Fault #1, while Fault #2 is a pole-to-ground fault [29]. The aircraft grounding method employed in this paper is based on a current return network (CRN) formed by the traditional metallic aircraft structure, with additional cables where required, thus ensuring a low electrical impedance (max. 0.1 to 0.2 ohms) [7], [30].

1) FCL mode (Fault #1):

When the system is subjected to a pole-to-pole fault current at the propulsion side, the SMES-FCL works in the FCL mode to limit the high current, as shown in Fig. 3(b). The fault lasts for 100 ms, from 5.0 s to 5.1 s. The current in the main feeder is shown in Fig. 4(a) in three cases: With and without the SMES-FCL device and with the separate SMES and FCL devices. Without the SMES-FCL, the current increases dramatically, whereas with the combined SMES-FCL, the FCL is able to limit the current to almost twice the rated current in few milliseconds. Fig. 4(b) shows the voltage at the generation side; without the SMES-FCL, the voltage drops to almost 0.23 pu of the nominal voltage, whereas with the SMES-FCL, the voltage is maintained above 0.86 pu. The generator speed is maintained above 0.98 pu of the nominal speed with the SMES-FCL; however, the speed drops to almost 0.94 pu of the nominal speed without the SMES-FCL device, as shown in Fig. 4 (c). It is noticeable that the separate FCL device works slightly faster than the combined SMES-FCL, but that is due to the latter using. switches. For all results in this section, the circuit breakers do not trip, showcasing the performance of the SMES-FCL device.



(a)

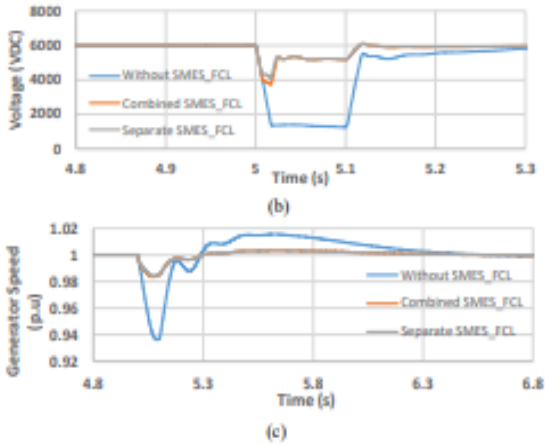


Fig. 4: Pole-to-pole fault on the propulsion side Fault #1 (a) Current without SMES-FCL, with combined SMES-FCL, and with separate SMES-FCL, (b) Voltage without SMES-FCL, with combined SMES-FCL, and with separate SMES-FCL, (c) Generator speed without SMES-FCL, with combined SMES-FCL, and with separate SMES-FCL

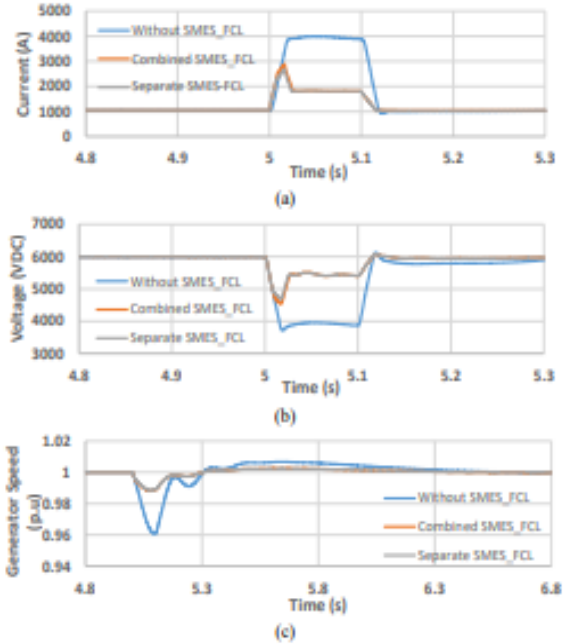


Fig. 5: Pole-to-ground fault on the propulsion side Fault #1 (a) Current without SMES-FCL, with combined SMES-FCL, and with separate SMES-FCL, (b) Voltage without SMES-FCL, with combined SMES-FCL, and with separate SMES-FCL, (c) Generator speed without SMES-FCL, with combined SMES-FCL, and with separate SMES-FCL.

Fig. 5 shows the effect of a pole-to-ground fault at the location of Fault #1 on the current, the bus voltage, and the generator speed in the same three cases explored in Fig. 4. It is clear that these effects are larger in magnitude during a pole-to-pole fault than in the pole-to-ground fault due to the higher potential voltage in the pole-to-pole fault.

2) SMES mode (Fault #2):

If the fault current occurs on the generation side, the SMES-FCL works in the SMES mode to maintain the voltage at the required level and maintain the propulsion system speed at the desired speed. When both the voltage and current drop at the DC-link, the SMES-FCL works as a SMES by discharging current to supply the propulsion system. The system was subjected to a pole-to-ground fault at the position of Fault #2, as shown in Fig. 1. The fault lasts for 100 ms from 5.0 s to 5.1s. The system works in the discharged mode, as shown in Fig. 3 (a). The SMES is able to maintain the voltage at the required level and the motors' speed at the reference speed. Fig. 6 (a) shows the speed of motor MR3 in the three different cases. Fig. 6 (b) shows the voltage at the DC-link in the three different cases. When the voltage dropped due to the fault current, the SMES discharged within few milliseconds as shown in in Fig. 6 (c). Here, the combined SMES-FCL and the separate devices act in the same way with no additional delay since the additional switches (S1-S6) are not used in this scenario.

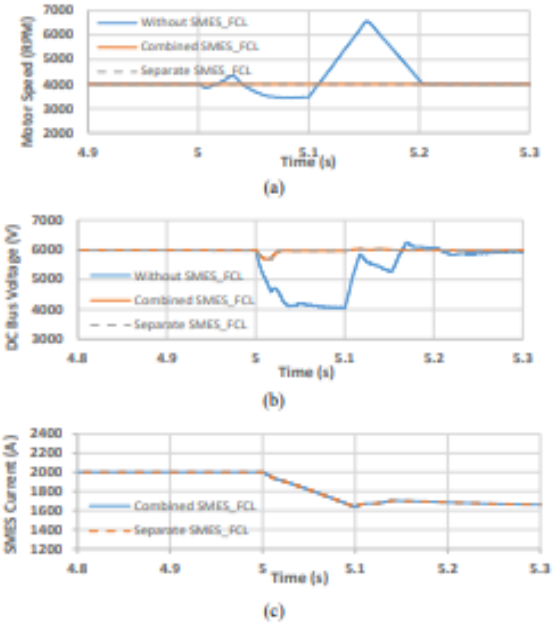


Fig. 6: Pole-to-ground fault on the generation side Fault #2 (a) Propulsion motor speed of MR3 without SMES-FCL, with combined SMES-FCL, with separate SMES-FCL, (b) Voltage without SMES-FCL, with combined SMES-FCL, and with separate SMES-FCL, (c) SMES current with combined SMES-FCL and with separate SMES-FCL.

V. Conclusions

This paper proposed the use of multifunction superconducting coils in the EA using a novel control technique. The proposed SMES-FCL can reduce the weight as well as the cost of EA by using the same coils in different operation modes. However, one of the potential negative side-effects of the combined SMES-FCL is the complexity of the design. Also, the SMES and FCL can work simultaneously when they are separate, whereas it is not possible in the combined device. And finally, the separate SMES and FCL can respond to faults slightly faster than the combined SMES-FCL due to the use of switches in the combined device.

The SMES-FCL device has been tested in three different fault scenarios. In the FCL mode, the SMES-FCL device was able to reduce the fault current from 7 times to almost twice the rated current within a few milliseconds, maintaining the voltage at above 0.86 pu of the nominal voltage, instead of 0.23 pu without the SMES-FCL device, and maintaining the generator speed at above 0.98 pu, instead of 0.94 pu without the SMES-FCL device. In the SMES mode, the SMES-FCL device was able to maintain the propulsion system speed at the required speed and the voltage at the DC-link at the reference voltage.

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Appendix C; Paper #3

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Analysing Faults and SFCL Response in Electric Aircraft

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Abstract. Aircraft technology moves towards electrification in order to achieve environmentally friendly goals. However, one of the main challenges facing the electrification of aircraft technology is the weight of the electric devices necessary for operating a fully electric aircraft. The National Aeronautics and Space Administration (NASA) proposed the use of the superconductive technology in electric aircraft (EA) to overcome this challenge in addition to its other benefits. The proposed EA is called N3-X and it has an on-board DC superconducting network including a superconducting fault current limiter (SFCL). The SFCL is a self-mechanism device that very effectively limits the current within a few milliseconds, thus improving the stability of the system. As the grounding of this network is different from traditional networks, analysing the behaviour of different fault types and how to manage them becomes critical. In this paper, one set of the EA's systems (one generator, AC/DC rectifier and four motors with their DC/AC variable frequency drives) has been modelled in MATLAB/Simulink environment to carry out the fault analysis and to demonstrate the effect of the SFCL on this network under different types of faults.

1. Introduction

As concerns regarding global warming and air pollution grows around the world, several organisations and companies started acting towards a healthier and cleaner environment. The National Aeronautics and Space Administration (NASA) and the Advisory Council for Aviation Research and Innovation in Europe (ACARE) have set goals to reduce carbon dioxide (CO_2) and nitrogen oxide (NO_x) emissions, as well as the external noise levels of commercial aircraft. These environmental goals are shown in Table 1 and are relative to the levels from the 2000 [1–3].

TABLE I
NASA AND ACARE ENVIRONMENTAL GOALS

Category	ACARE 2020	ACARE 2050	NASA N+2 ~2020	NASA N+3 ~2030
CO_2 reduction	50%	75%	-	-
NO_x reduction	80%	90%	75%	80%
Noise reduction	50%	65%	-42 dB	-71dB
Fuel burn	50%	-	50%	60%

Because the current hydraulic, pneumatic, and mechanical actuators in conventional aircraft are relatively inefficient (~40%) [4], moving towards Electrical Aircraft (EA) is a promising solution to achieve environmentally friendly goals such as the ones in Table 1 [5]. One of the obvious solutions is the use of batteries as the energy source. Currently, few electric aircraft operate battery-only systems, including the E-Fan. E-Fan was a two-seat fully electric aircraft powered by a battery-only system produced by Airbus for pilot training and two-seat touring in 2014 [6]. However, while it is possible to fly ultra-light and small-size aircraft with battery-only systems, it is not possible to fly commercial aircraft with over 100 passengers with battery-only systems due of the low energy density (kWh/kg) of batteries 320 [7]. Airbus, along with its partners Rolls-Royce and Siemens, have started a new hybrid-electric propulsion project for commercial aircraft, named the E-Fan X. The testbed of the E-Fan X is based on replacing one of its four turbofans with a 2 MW electric motor, and the E-Fan X is anticipated to fly in 2020 [8]. Another such project was the UK government-funded Distributed Electrical Aerospace Propulsion (DEAP) project where Airbus, Rolls Royce, and Canfield University investigated the feasibility of distributed propulsion systems in aircraft by using two gas-driven high temperature superconducting (HTS) turbo-generators and eight HTS motor-driven fans to produce the require thrust [9].

NASA introduced the concept of Turboelectric Distributed Propulsion (TeDP) systems in 2005. The main idea of TeDP is relocating the gas turbine engines away from the propulsors, resulting in the EA's power architecture to look like a small microgrid with a number of gas turbine engines and motors connected to fans or propellers, allowing for the hybridization of energy sources and the implementation of superconducting fault current limiters (SFCL) to improve the system's performance [10].

The most notable EA concept is NASA's N3-X and was proposed under NASA's Research and Technology for Aerospace Propulsion (RTAPS) initiative [11]. N3-X is a DC microgrid on-board, which consists of sixteen motors, four generators, and several electrical devices including rectifiers, inverters, circuit breakers, and SFCL [10]. A SFCL is a self-mechanism device that provides very effective current limitation within a few milliseconds of a fault occurring [13–15]. When the current exceeds the critical current ($I_{critical}$), the resistivity of the superconducting coil increases quickly, reducing the system's maximum fault current.

The on-board installed electrical power systems and the overall network of the electric aircraft face several design challenges, including the grounding of this network. In order to carry out the fault analysis and to demonstrate the effect and importance of the SFCL in the EA, one set of the EA's systems, as shown in Fig. 1, has been modelled in MATLAB/Simulink environment.

2. System Description

The N3-X TeDP power system architecture, the Inner Bus Tie Concept (IBTC), proposed by NASA [10], was chosen as the platform for carrying the fault analysis of the EA and the SFCL response. In this paper, one set of the power system architecture of the N3-X has been modelled, with four motors (1.86 MW each) and one generator (14.91 MW) as shown in Fig. 1, instead of the full sixteen motors and four generators [10]. The system components are shown in Table II and Fig. 1.

TABLE II

THE DESIGN PARAMETERS OF THE EA

Parameter	Quantity	Value
Generator	1	14.91 MW, 6 kV
Motor	4	1.86 MW
AC/DC Rectifier	1	14.91 MW
DC/AC Inverter	4	1.8 MW
SFCL	4	I_{rate} = 320 A, $I_{critical}$ =900 A
	1	I_{rate} = 1.28 kA, $I_{critical}$ =2.7 kA

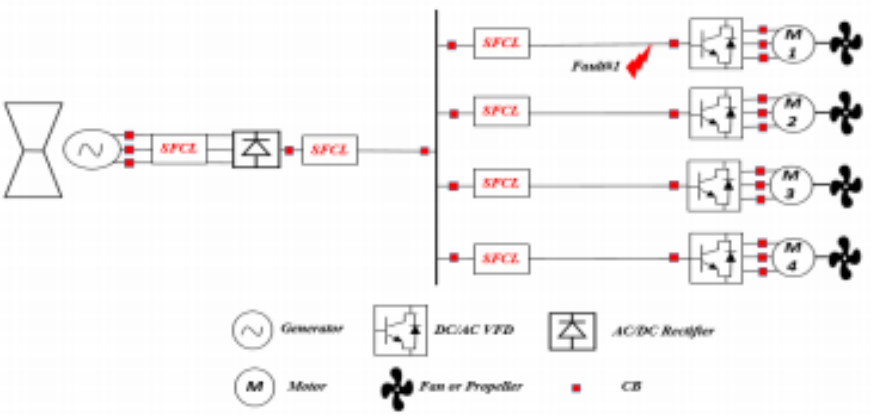

Fig. 1: One set of the EA with one generator, AC/DC rectifier, DC/AC inverter, four motors.

The ratings of the generator, motors, and converters are based on the data of the aircraft proposed by NASA [10] The propulsion system is required to produce 22.5 MW for maximum thrust during take-off [15]. Because each motor can produce 1.86 MW thrust, at least 12 motors are required to work at the same time to ensure safe operation. The voltage DC-link is rated at 6 kVDC, as recommended by NASA [16]. In the proposed architecture, propulsion is provided by surface permanent magnet synchronous motors (SPMSM), which were chosen for their high power density and efficiency [17], the stator phase resistance is 24.21 mΩ. A non-salient, synchronous machine is chosen to model the characteristics of the generator with a stator resistance of 26.86 mΩ. The on-state resistance of the IGBTs used in the converter is estimated to be 1.5 mΩ. The fault current will be applied on the branch feeder as shown in Fig. 1. Different types of faults will be demonstrated: pole-to-pole, pole-to-ground with low grounding impedance.

3. Superconducting Fault Current Limiter (SFCL)

A SFCL is a self-mechanism electrical device which limits the fault current when a fault occurs, all within a few milliseconds, thus allowing the electrical network's protection system (switchgear, circuit breakers, etc.) to operate safely [18].

Because the EA has an on-board compact electrical network with high fault current levels, this level of fault current, if not properly managed, may exceed the maximum ratings of the protection systems, such as switchgears or circuit breakers, and consequently permanently damaging several devices such as generators, motors and cables via burnout. However, the use of the SFCL can reduce the fault current level to ensure safe operation for the protection system of the electrical network.

In general, SFCLs are classified into two main types: Resistive SFCL (R-SFCL) and Inductive (I-SFCL). Because the I-SFCL is heavier and more complex than the R-SFCL [19,20]and the weight is a crucial point in EA design, the focus of this paper will be on the R-SFCL type. The schematic circuit of a traditional R-SFCL is shown in Fig. 2.

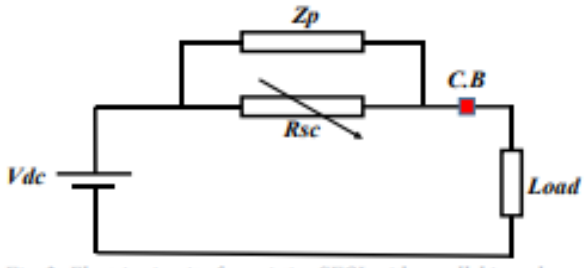

Fig. 2: Electric circuit of a resistive SFCL with parallel impedance

The two most common materials used to construct the SFCL are Yttrium Barium Copper Oxide (YBCO) and Bismuth Strontium Calcium Copper Oxide (BSCCO); both categorized as high temperature superconductors (HTS). In this study, YBCO is chosen to be the material of the R-SFCL for its better performance [20,21].

Two variables that control the behavior of the SFCL are the critical temperature and critical current density. The resistance of the R-SFCL can be calculated by the following equations:

$$J_c(T) = J_{co}\left(\frac{(T_c - T(t))^a}{(T_c - T_o)^a}\right) \qquad T_o < T < T_c \tag{1}$$

$$\rho_{HTS} = \frac{E_c}{J_c(T)}\left(\frac{J}{J_c(T)}\right)^{N-1} \qquad T < T_c\,, \quad J > J_C \tag{2}$$

$$\rho_{cu} = (0.0084T - 0.4603) \times 10^{-8} \qquad T > T_c \tag{3}$$

$$R_{sc} = \rho_{sc}\,\frac{l}{A} \tag{4}$$

$$T(t) = T_o + \frac{1}{C_p}\int_0^t Q_{sc}(t)dt \tag{5}$$

$$Q_{sc}(t) = P_{diss}(t) - P_{cooling}(t) \tag{6}$$

where J_{co} is the critical current density of the tape at the initial temperature. The initial temperature is the normal operation temperature, assumed here as the boiling temperature of liquid nitrogen (77 K). a is the density exponent and is equal to 1.5, which is applicable to YBCO material [22]. The critical temperature of YBCO T_c is equal to 92 K. When the current is less than the critical current of the YBCO material, the YBCO tape works in a superconductive state, meaning it has zero resistance, $\rho_{sc} = 0$. However, when the current exceeds the critical current value, the resistivity of the HTS layer increases sharply, according to Eq. 1. $Ec = 1$ μV/cm, which represents the electrical field. For the YBCO tapes, the N value ranges between 21 and 30. Eq. 2 is only valid when the temperature is less than the critical temperature and the current density is higher than the critical current density $J > J_C$. Under these two conditions the YBCO tape resistivity is equal to the resistivity of the superconducting layer, $\rho_{sc} = \rho_{HTS}$. However, when the temperature exceeds the critical temperature, the resistivity of the HTS layer becomes higher than the resistivity of the copper stabilizer, thus most of the current goes through the copper layers and $\rho_{sc} = \rho_{cu}$. The resistivity of the copper layers depends on the temperature, as shown in Eq. 3. The resistance of the superconducting tape can be obtained from the resistivity of the HTS layer ρ_{HTS} from Eq. 2, and the resistivity of the copper stabilizer ρ_{cu} from Eq. 3, respectively. The HTS tape resistance is calculated using Eq. 4 where l is the length of the tape and A is the cross-sectional area of the tape. The temperature of the tape is calculated through Eq. 5 where Q_{sc} is the corresponding net power in the tape and C_p is the specific heat capacity of the material, which describes the amount of heat needed to increase the temperature of the material by one degree. In Eq. 6, $P_{diss}(t)$ represents the dissipated power in the superconducting tape and $P_{cooling}(t)$ is the cooling power representing the energy absorbed by the cooler. $P_{cooling}(t)$ reduces the temperature rise during a fault and brings the tape to a superconductive state after the fault.

TABLE III
THE DESIGN PARAMETERS OF SFCL

Parameter	Value
Critical Current (A)	300
Width (mm)	12
Total thickness (mm)	0.1
Copper stabilizer thickness (μm)	40
Length of YBCO tape (m)	233
Number of wires in parallel	3
Rated voltage (kV)	6
Resistance (Ω) @100 K	0.614
Resistance (Ω) @300 K	3.34

This paper focuses on the design of the four SFCLs on the branches shown in Fig. 1. The parameters of the SFCL are determined in Table III based on the initial fault analysis. The wire used in this paper is a 12 mm wide and 0.1 mm thick YBCO wire with a minimum critical current of 300 A (SCS12050) [23]. To build a 3.34 Ω @300 K YBCO tape with a copper stabilizer, three parallel 10 Ω @ 300 K tapes are used, each consisting of 233 m of superconducting tape. The critical current rating of this SFCL is 900 A.

4. Electric Aircraft Grounding System

All electrical systems must be grounded for several reasons, including enabling the detection of ground faults, as well as protecting human life and equipment, but the main goal is to redirect the vast amount of current during fault scenarios. In traditional electrical networks, the metallic part of equipment is connected to the earth. This is to provide an alternate high-voltage discharge path on the outside if the equipment's insulation fails for any reason as shown in Fig. 3(a). If the equipment is not earthed, these dangerous voltages can be transferred to anyone who touches it, resulting in an electric shock [24], [25]. However, connecting an aircraft to the earth is not possible at 30,000 feet, and thus the airframe (fuselage) is used for the grounding system instead.

The airframe can be made from different materials, including aluminum alloys as shown in Fig. 3(b). Because aluminum alloys are good conductors, the airframe can act as the traditional grounding (earth) which could be used as grounding, bonding, voltage reference and a current return path due to its high electrical conductivity, thereby reducing the number of wires on-board the aircraft by half [26].

As the power system architecture used in this paper is a DC power system based on the proposed N3-X architecture, the grounding system will be based on a positive pole, a negative pole as a return path, and the airframe as a ground, as shown in Fig. 3(c). The pole-to-pole fault is not affected by the different airframe or grounding technique because the return path of the fault is the negative pole. However, pole-to-ground faults are affected by changes in the airframe or the grounding technique.

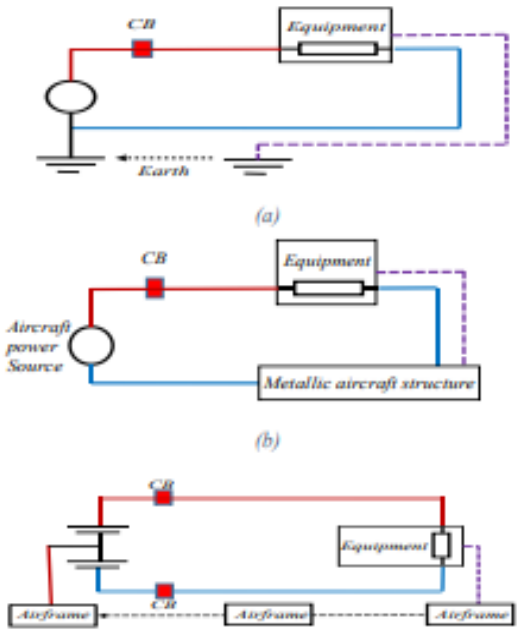

Fig. 3: Electric Grounding Systems: (a) Traditional, (b) Metallic Airframe, (c) DC-based EA

5. Simulation Results & Discussion

In order to investigate the fault behaviour in EA, the power system architecture of the EA shown in Fig. 1 is modelled in the MATLAB/Simulink system environment. The distance from the VSC to the DC bus is estimated to be 40 m and the distance from the DC bus to the motor's VFD is 5 m based on [10]. The resistance and inductance from the VSC to the fault position (assumed here to be at the end of the DC line as shown in Fig. 1) is 4.088 mΩ and 25.22 uH based on [27]. The DC-link capacitor is calculated to be 40 mF to ensure stable voltage on the DC-link. Two different types of faults are demonstrated in this section: a pole-to-pole fault and a pole-to-ground with low impedance grounding (0.1 Ω). A pole-to-pole fault is the most hazardous fault types due to the high voltage level between the positive and negative pole (+3 kV to -3 kV) and the low line impedance. On the other hand, a pole-to-ground fault occurs when either the positive or negative pole is connected directly to the ground. The most common type of short circuit is a pole-to-ground fault, yet it is not as critical as a pole-to-pole fault [28] ,[29]. For all results in this section, the circuit breakers do not trip, showcasing the performance of the SFCL device.

5.1 Case Study 1: Pole-to-Pole Fault

A pole-to-pole fault is applied at the location "Fault #1" on the feeder of the motor M1 shown in Fig. 1 for 100 milliseconds from t=2.0 s to t=2.1 s. Fig. 4(a) shows the voltage on the DC bus with and without SFCL, while the current of the feeder is shown in Fig. 4(b) with and without SFCL. Fig. 4(c) shows the AC voltage of the variable frequency drive (VFD) on the non-faulted branches, without SFCL. To show the effect of the fault on motors on the non-faulted branches, the motor speed of M4 from Fig. 1 is shown in Fig. 4(d) with and without SFCL.

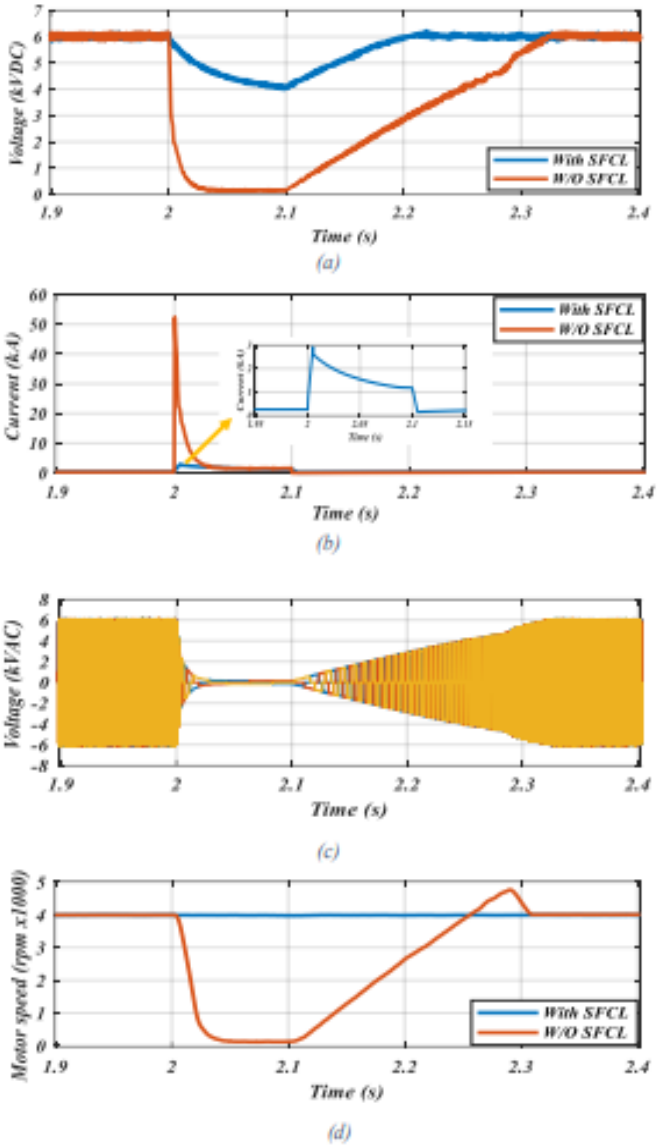

Fig. 4: Pole-to-pole fault current on the propulsion side at Fault#1 (a) Voltage at the DC bus with and without SFCL (b) Current at the motor branch with and without FCL (c) AC voltage on the non-faulted branches without SFCL (d) Motor speed M4 with and without SFCL.

The rated voltage of the DC bus is 6 kVDC. When the fault current occurred at t=2.0 s, the voltage of the DC bus dropped from 6 kVDC to almost zero without SFCL. With the SFCL however, the voltage only dropped to 4 kVDC for just few milliseconds. The rated current of each branch is 320 A. When the fault occurred, the current rose to almost 52 kA without the SFCL, whereas with the SFCL, the current was limited to 3 kA. The AC voltage of the VFD connected to motors on the non-faulted branches is shown in Fig. 4(c). When observing the speed of the motors on the non-faulted branches (specifically M4 here), the SFCL was able to maintain the desired speed, while the motor fed the fault then went into overdrive before eventually stabilising without the SFCL as shown in Fig. 4(d).

5.2 *Case Study 2: Pole-to-Ground Fault with Low Impedance Grounding*

A pole-to-ground fault is applied at "Fault #1" as shown in Fig. 1 with low impedance grounding (0.1 Ω) for 100 milliseconds from t=2 s to t=2.1 s. Fig. 5(a) shows the DC bus voltage with and without the SFCL, while the current of the faulted branch is shown in Fig. 5(b) with and without SFCL. Fig. 5(c) shows the AC voltage of the VFD on the non-faulted branches, without SFCL. The motor speed of M4 from Fig. 1 is shown in Fig. 5(d) with and without SFCL.

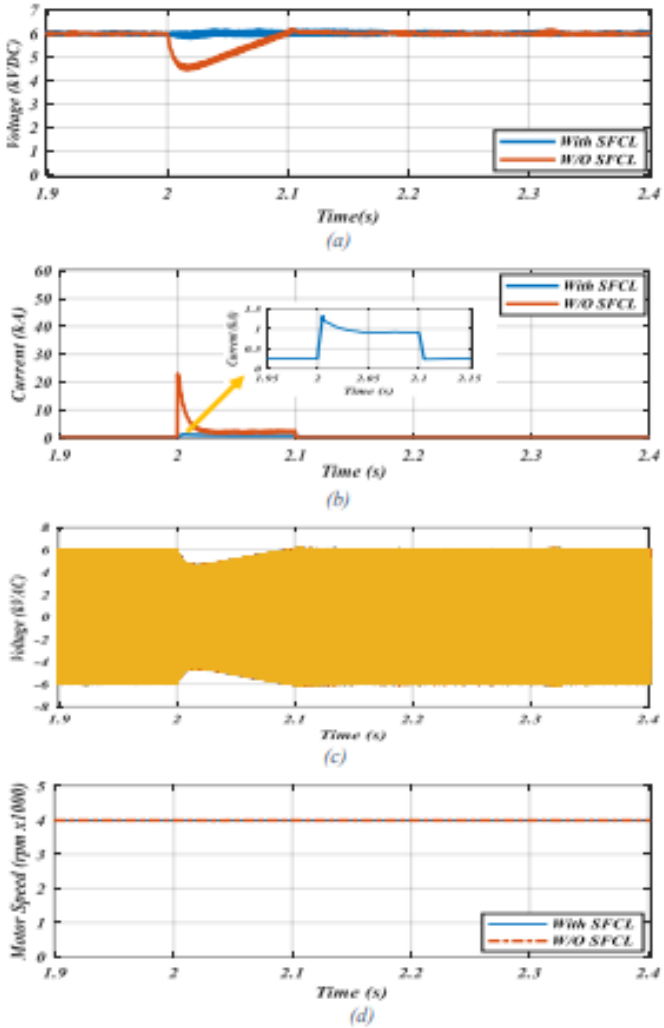

Fig. 5: Pole-to-ground fault current with low ground impedance (0.1 ohm) on the propulsion side at Fault#1 (a) Voltage at the DC bus with and without FCL (b) Current at the motor branch with and without SFCL (c) AC voltage on non-faulted branches without SFCL (d) Motor speed M4 with and without SFCL.

The voltage drop of the pole-to-ground fault was lower and shorter in time than the pole-to-pole fault for two reasons. Firstly, the voltage difference is half of that in the pole-to-pole fault (+3 kV to ground compared to +3 kV to -3 kV, respectively). Secondly, the DC voltage controller in the AC/DC rectifier-imposed overvoltage on the healthy pole to compensate for the voltage drop on the faulty pole, thus maintaining the overall voltage of the DC bus at the required level. When the fault occurred, the current rose to almost 22 kA without the SFCL, whereas with the SFCL, the current was limited to 1.4 kA. The AC voltage of the VFD is shown in Fig. 5(c). Because the voltage drop of the main bus was small and short in time, the speed of the motor M4 remained stable even without the SFCL.

Both the pole-to-pole and pole-to-ground faults are very hazardous for the system. In the pole-to-pole fault, the voltage difference is 6 kV compared to 3 kV in the pole-to-ground. The resulting drop of the main DC bus's voltage was high, dropping from 6 kV to almost zero, which affected the stability of the other motors on the non-faulted branches as shown in Fig. 4(d). Meanwhile, in the pole-to-ground fault, the voltage drop was small, and the AC/DC rectifier-imposed overvoltage on the healthy pole, thus reducing the voltage on the faulty pole and the resulting fault current. These factors combined with the short duration of the fault resulted in the pole-to-ground fault not affecting the stability of the non-faulted branches. Thus, the SFCL is important for both types of faults to reduce the fault current level and to support the protection system, with it being especially critical during the pole-to-pole fault.

6. Conclusion

This paper investigated and analyzed the behavior of a proposed power system architecture of EA based on NASA N3-X during different fault current scenarios. Different types of faults were applied at the feeder that feeds the EA motor: pole-to-pole, and pole-to-ground with low impedance grounding. In addition, the SFCL responses were demonstrated to show the effectiveness of the SFCL on the system in each scenario. Because the EA has a compact electrical network on-board operating at a high voltage level and a small impedance line, the current rose from 320 A to almost 52 kA during the pole-to-pole fault with the SFCL absent. The SFCL was able to limit the fault current to around 3 kA, which is only 5.7 % of the fault current without it. The fault current of the pole-to-ground fault with low impedance grounding reached almost 22 kA, which is lower than during the pole-to-pole fault. That was due to the lower voltage difference and the voltage controller which reduced the voltage on the faulty pole and increased the voltage on the healthy pole, thus reducing the fault current. The SFCL in that case was able to again limit the fault current to around 1.4 kA which is 6.36% of the fault current in this scenario. In either case, the presence of the SFCL was critical in avoiding the excessive increase in fault current which would lead to permanent damage to other parts of the system. Additionally, that means that the rating of the circuit breaker necessary to interrupt such a fault would be much lower and would thus be smaller, saving valuable space on the aircraft for other components, passengers, luggage, and so on.

7. Acknowledgments

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